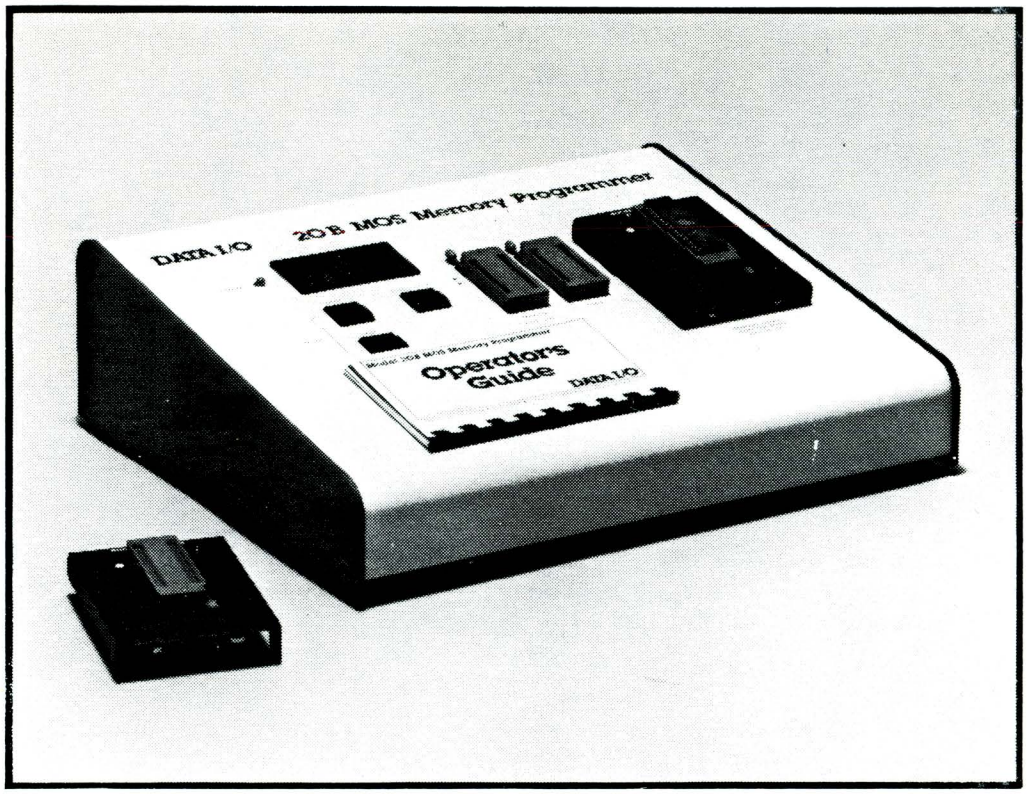

MODEL 20B
MOS MEMORY PROGRAMMER
WITH REMOTE CONTROL

REV A SEPT 81 **10-990-0011-001**

Data I/O Corporation
P.O. Box 308/1297 N.W. Mall
Issaquah, WA 98027

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Data I/O reserves the right to make changes to this document without notice at any time.

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SECTION 1
INTRODUCTION

1.1 BASIC DESCRIPTION

The Data I/O Model 20B MOS Memory Programmer is a portable programmer/duplicator that is capable of stand-alone or remote operation. As a stand-alone duplicator, the Model 20B uses software to generate the programming algorithms for most 24- and 28-pin NMOS EPROMs currently available for commercial use. In addition, 40-pin single chip microcomputers can be programmed using the remote control mode with an optional socket adapter. Under remote control, programming data comes from a remote instrument and resides in the programmer's 2K RAM.

1.1.1 STAND-ALONE OPERATION

The Model 20B incorporates a series of operational checks to insure that all PROMs are programmed correctly. Prior to each programming operation, the Model 20B performs tests to eliminate all possibilities of error, both in the PROMs and in the programmer itself. If any error occurs, the Model 20B halts operation to display a unique "Error Code" that pinpoints the error. If critical programming voltages drift out of tolerance, a diagnostic mode allows the operator to measure those voltages at the socket and readjust them.

The Model 20B's 4-character LED display reports the programmer's status to the operator at all times, including the operating modes selected, the device selected for programming, the sum-check* of the programmed data, and Error Codes.

Microcomputers cannot be programmed from the front panel.

* Sum-check is explained in the Glossary, Section 8.

1.1.2 REMOTE OPERATION

Under remote control, preoperational checks, data transfers, and programming are all commanded from a CRT terminal. Status and error messages appear on the CRT screen. Data may be entered to the 2K RAM directly from a data terminal. Microcomputers can only be programmed with remote control operation. See section 3.5.

1.2 PROGRAMMING APPLICATIONS

Table 1-1 lists the PROMs and microcomputers which the Model 20B currently programs. As new, generically similar PROMs come into the market, Data I/O will publish *customer notices* to announce new programming capabilities for the Model 20B.

1.3 HOW THE MODEL 20B FUNCTIONS

The Model 20B programs by reading each address of the PROM in the Master Socket to determine which bits in it are programmed, and then applying programming pulses to the same bits at the corresponding address in the blank PROM. These pulses are applied in sequence; all bits to be programmed at one address are pulsed simultaneously the required number of times, and then the programmer goes to the next address. The number of pulses applied at each address is specified by the PROM manufacturer.

The programming routine is followed automatically by a verification routine, which consists of a bit-by-bit comparison of the data in both PROMs. The Model 20B signals an error if the data in the PROMs is not identical.

Under remote operation, programming data resides in the 2K RAM. No master PROM is used. For PROMs larger than 2K x 8 bits, the Model 20B employs 2 methods of programming by automatic, sequential input-then-program routines. The Model 20B can also program these large PROMs or 40-pin, single chip microcomponents when under remote control from a computer.

1.4 SPECIFICATIONS

1.4.1 MAJOR COMPONENTS

Control Electronics. Microprocessor-controlled (type 6802)

Programming Electronics. Programming parameters are software-controlled. All voltages are current-limited and monitored to meet PROM manufacturers' programming specifications.

1.4.2 ELECTRICAL REQUIREMENTS

Operating Voltages. 100, 120, 220, or 240 VAC, within +5% or −10%, grounded, single phase.

Frequency Range. 50 to 60 Hz

Power Consumption. 30 W nominal

Fuse Protection: An AC line fuse accessed from the back panel. Unscrew the fuse cover on the back panel to remove the line fuse.

Fuse rating: .5 A for 100 and 120 V units
.25 A for 220 and 240 V units

Five power supply fuses, F1 through F5, are located on the Power Supply Card, part number 702-0072-001. To access those fuses, remove the cover according to paragraph 2.2.1. Locate F1 through F5 on the Power Supply Card.

Fuse ratings: 125 V, 2A (fast blow)

1.4.3 PHYSICAL AND ENVIRONMENTAL SPECIFICATIONS

Dimensions. 31.2 cm wide x 26.9 cm high x 10.4 cm deep (12.3" x 10.6" x 4.1")

Table 1-1. Programming Applications of the Model 20B

Array Size Technology	Pinout	PROM Part Number	PROM Code Family and Pinout Codes Model 20A Rev. Letter*
Advanced Micro Devices			
1024x8 MOS	24	2708	2708/2127
2048x8 MOS	24	4716	2516/1923
Electronic Arrays			
1024x8 MOS	24	2708	2708/2127
2048x8 MOS	24	2716	2516/1923
Fairchild Semiconductor			
1024x8 MOS	24	2708	2708/2127
Fujitsu			
1024x8 MOS	24	8518 (2708)	2708/2127
2048x8 MOS	24	8516 (2716)	2516/1923
Hitachi			
2048x8 MOS	24	462716	2516/1923
2048x8 MOS	24	48016	4816/3323
4096x8 MOS	24	462532	2532/1925
4096x8 MOS	24	462732	2732/1924
Intel			
512x8 MOS	24	2704/8704	2704/2126
1024x8 MOS	24	2708/8708	2708/2127
1024x8 MOS	24	2758	2508/1922
1024x8 MOS	24	2758 S1865	2508/1922†
1024x8 MOS	40	8741	8741/5659 ††
1024x8 MOS	40	8748	8748/5256 ††
1024x8 MOS	40	8748H	8749/5057†
2048x8 MOS	24	2716	2516/1923
2048x8 MOS	40	8749H	8749/5057 ††
2048x8 MOS	40	8755A	8755/4755 ††
4096x8 MOS	24	2732	2732/1924
4096x8 MOS	24	2732A	732A/2724
4096x8 MOS	40	8751	8751/5458 †††
8192x8 MOS	28	2764	764n/3533
Intersil			
1024x8 MOS	24	2708	2708/2127
Maruman Integrated Circuits			
2048x8 MOS	24	2716	2516/1923
Mitsubishi			
1024x8 MOS	24	58732S (2708)	2708/2127
1024x8 MOS	24	2708	2708/2127
2048x8 MOS	24	2716	2516/1923
Mostek			
2048x8 MOS	24	2716	2516/1923
8192x8 MOS	28	2764	2764/4539
Motorola			
1024x8 MOS	24	68708/2708L	2708/2127
1024x8 MOS	24	2708P	2708/2127
2048x8 MOS	24	TMS2716	2716/2328
2048x8 MOS	24	MCM2716	2516/1923
4096x8 MOS	24	2532	2532/1925
4096x8 MOS	24	68732-0	7320/2544
4096x8 MOS	24	68732-1	7321/2545
8192x8 MOS	24	68764	8764/2529
National Semiconductor			
1024x8 MOS	24	2708	2708/2127
1024x8 MOS	24	2758A	2508/1922
1024x8 MOS	24	2758B	2508/1922†
2048x8 MOS	24	2716	2516/1923
4096x8 MOS	24	2532	2532/1925
4096x8 MOS	24	2732	2732/1924
Nippon Electric Co., Ltd.			
2048x8 MOS	24	2716	2516/1923
Oki			
2048x8 MOS	24	2716	2516/1923
Signetics			
1024x8 MOS	24	2708	2708/2127
Texas Instruments			
1024x8 MOS	24	2508	2508/1922
1024x8 MOS	24	2708/27L08	2708/2127
2048x8 MOS	24	2716	2716/2328
2048x8 MOS	24	2516	2516/1923
4096x8 MOS	24	2532	2532/1925
8192x8 MOS	28	2564	2564/3130
Toshiba			
512x8 MOS	24	321	2704/2126
1024x8 MOS	24	322	2708/2127
2048x8 MOS	24	323	2516/1923

* If there is a revision letter in this column, it specifies the earliest version of the Model 20B that will program the PROM per its manufacturer's latest specifications. You can use this column to document revisions. Data I/O customer notices will provide information on Model 20B updates.

† This PROM can be programmed only in remote control. Before sending the Program (P) command, send the Set Block Size command (;) and the Set Begin Device command (:), specifying hex value 400 for each command.

†† These devices are programmed in remote control only.

††† This device is programmed in remote control only. Device Commands T, B, L, P and V operate on only the lower half of the EPROM device array. To access the upper half of the device, set the Set Begin Device (:) Command, at hex address 800.

Table 1-1. Programming Applications of the Model 20B

Array Size Technology	Pinout	PROM Part Number	PROM Code Family and Pinout Codes	Model 20B Rev. Letter*
Advanced Micro Devices				
1024x8 MOS	24	2708	2708/2127	A
2048x8 MOS	24	4716	2516/1923	A
Electronic Arrays				
1024x8 MOS	24	2708	2708/2127	A
2048x8 MOS	24	2716	2516/1923	A
Fairchild Semiconductor				
1024x8 MOS	24	2708	2708/2127	A
Fujitsu				
1024x8 MOS	24	8518 (2708)	2708/2127	A
2048x8 MOS	24	8516 (2716)	2516/1923	A
Hitachi				
2048x8 MOS	24	462716	2516/1923	A
2048x8 MOS	24	48016	4816/3323	A
4096x8 MOS	24	462532	2532/1925	A
4096x8 MOS	24	462732	2732/1924	A
Intel				
512x8 MOS	24	2704/8704	2704/2126	A
1024x8 MOS	24	2708/8708	2708/2127	A
1024x8 MOS	24	2758	2508/1922	A
1024x8 MOS	24	2758 S1865	2508/1922†	A
1024x8 MOS	40	8741	8741/5659	A
1024x8 MOS	40	8748	8748/5256	A
1024x8 MOS	40	8748H	8749/5057	B
2048x8 MOS	24	2716	2516/1923	A
2048x8 MOS	40	8749H	8749/5057	B
2048x8 MOS	40	8755A	8755/4755	A
2048x8 MOS	24	2816	2816/3723	B
4096x8 MOS	24	2732	2732/1924	A
4096x8 MOS	24	2732A	732A/2724	A
4096x8 MOS	40	8751	751L/751H/5358††	B
8192x8 MOS	28	2764	764n/3533	A
8192x8 MOS	28	2764	2763/7933•	B
Intersil				
1024x8 MOS	24	2708	2708/2127	A
Maruman Integrated Circuits				
2048x8 MOS	24	2716	2516/1923	A
Mitsubishi				
1024x8 MOS	24	58732S (2708)	2708/2127	A
1024x8 MOS	24	2708	2708/2127	A
Mitsubishi (cont.)				
2048x8 MOS	24	2716	2516/1923	A
Mostek				
2048x8 MOS	24	2716	2516/1923	A
8192x8 MOS	28	2764	2764/4539	A
Motorola				
1024x8 MOS	24	68708/2708L	2708/2127	A
1024x8 MOS	24	2708P	2708/2127	A
2048x8 MOS	24	TMS2716	2716/2328	A
2048x8 MOS	24	MCM2716	2516/1923	A
4096x8 MOS	24	2532	2532/1925	A
4096x8 MOS	24	68732-0	7320/2544	A
4096x8 MOS	24	68732-1	7321/2545	A
8192x8 MOS	24	68764	8764/2529	A
National Semiconductor				
1024x8 MOS	24	2708	2708/2127	A
1024x8 MOS	24	2758A	2508/1922	A
1024x8 MOS	24	2758B	2508/1922†	A
2048x8 MOS	24	2716	2516/1923	A
4096x8 MOS	24	2532	2532/1925	A
4096x8 MOS	24	2732	2732/1924	A
Nippon Electric Co., Ltd.				
2048x8 MOS	24	2716	2516/1923	A
Oki				
2048x8 MOS	24	2716	2516/1923	A
Signetics				
1024x8 MOS	24	2708	2708/2127	A
Texas Instruments				
1024x8 MOS	24	2508	2508/1922	A
1024x8 MOS	24	2708/27L08	2708/2127	A
2048x8 MOS	24	2716	2716/2328	A
2048x8 MOS	24	2516	2516/1923	A
4096x8 MOS	24	2532	2532/1925	A
8192x8 MOS	28	2564	2564/3130	A
Toshiba				
512x8 MOS	24	321	2704/2126	A
1024x8 MOS	24	322	2708/2127	A
2048x8 MOS	24	323	2516/1923	A

* If there is a revision letter in this column, it specifies the earliest version of the Model 20B that will program the PROM per its manufacturer's latest specifications. You can use this column to document revisions. Data I/O customer notices will provide information on Model 20B updates.

† This PROM can be programmed only in remote control. Before sending the Program (P) command, send the Set Block Size command (;) and the Set Begin Device command (:), specifying hex value 400 for each command.

†† This device is programmed in two 2k blocks. Using front panel control 751L selects the lower 2k and 751H selects the upper 2k. Using remote control, the Begin Device Command selects the 2k block.

• Intel's 2764 device with fast programming algorithm.

DOCUMENT ADDENDUM

The information found in the Sections and pages listed in this addendum have been revised. Before using this manual, be certain to note these changes.

Your programmer software provides you with capability to program 27128 devices. Data I/O's 351A-069 socket adapter programs the 27128 and will be ready for delivery during the second quarter of this year. If you wish to order this socket adapter, contact your nearest Data I/O Service Center.

On page 1.2, table 1.1, of your Model 20B manual (10-990-0011) and on page 5 of your Operator's Guide (12-990-0011), please add the following to the list of Intel devices:

16384x8MOS	28	27128	7127/7951*
16384x8MOS	28	27128	7128/3551

*Intel's Int$_e$ligent Algorithm™

Weight. 3.7 kg (8.1 lb)

Operating Temperature Range. 0° to 40°C (32° to 104°F)

Storage Temperature Range. −40° to 55°C (−40° to 131°F)

Relative Humidity. 90% at 40°C (noncondensing)

1.5 PROGRAMMING ALGORITHMS

All Data I/O programming algorithms are approved by the manufacturers whose devices they program.

1.6 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use, but we suggest every three months, or more often if programming yields are low or the operating environment is dusty or excessively humid.

1.7 LIMITED WARRANTY

Data I/O warranties its equipment against defects in materials and workmanship. The warranty period on the Model 20B is one year and begins when you receive it.

The warranty card inside the back cover of this manual explains the warranty.

NOTE

To ship the programmer for service, package it according to the instructions in paragraph 2.6. Improper packing will void the warranty. For information regarding the proper return location and procedure, contact your local Data I/O representative.

1.8 SERVICE

Data I/O maintains Service Centers throughout the world. Each facility is staffed with factory-trained technicians to provide prompt, quality service. In addition to repairs, all Data I/O products are calibrated.

For more information about servicing your Data I/O products, contact your local Data I/O representative. A list of Data I/O service centers is included with this manual.

1.9 ORDERING

To place an order for equipment, contact your Data I/O sales representative.

Orders for equipment should contain the following information:

- Description of equipment. (See the latest Data I/O Price List or contact your sales representative for equipment and part numbers.)
- Quantity of each item ordered.
- Shipping and billing address of firm, including zip code.
- Name of person ordering the equipment.
- Purchase order number.
- Desired method of shipment.

SECTION 2
INSTALLATION

2.1 INTRODUCTION

Section 2 explains inspection, set-up and repackaging of the unit. Read it thoroughly before operating the unit.

2.2 INSPECTION

The Model 20B was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should therefore arrive free of any defect, without marks or scratches, and in perfect operating condition. Carefully inspect the unit for any damage that may have occurred in transit; if you note any damage or defect, file a claim with the carrier and notify Data I/O. Also check that the equipment listed in Table 2-1 is present.

2.3 DISASSEMBLING THE CASE

For operations that require access to components inside the unit, complete the following directions and refer to Figure 2-1.

1. Make sure the power is off.

2. Disconnect the AC power cord.

3. Turn the programmer upside-down and remove the 9 screws which connect the cover to the base.

4. Separate the cover from the base. For ease of access to components inside the unit, lay the cover upside-down beside the base, being careful not to stretch the 22-conductor flat cable.

Table 2-1. Supplied Equipment

PART	QUANTITY	DATA I/O PART NUMBER
Model 20B Programmer	1	
120 VAC		901-0011-001
100 VAC		901-0011-002
220 VAC		901-0011-003
240 VAC		901-0011-004
AC Power Cord	1	
120 VAC		416-1577
100 VAC		416-1577
220 VAC		416-0010
240 VAC		416-0010
Optional 40 Pin Socket Adapter	1	715-0094-001
Optional 40 Pin Socket Adapter	1	715-0095-001
Operation and Maintenance Manual	1	10-990-0011-001
Operator's Guide	1	12-990-0011-001

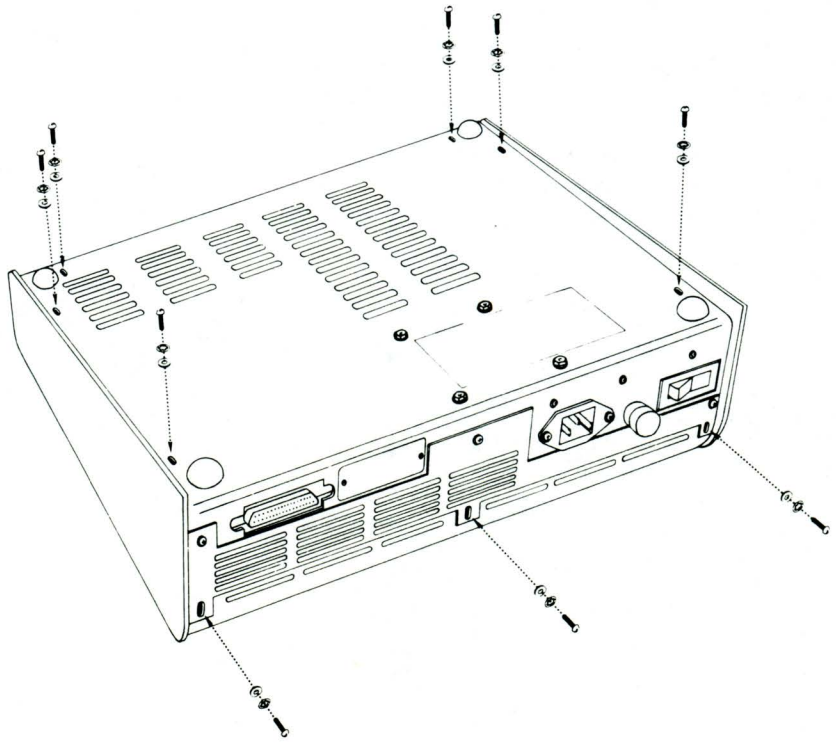


Figure 2-1. Disassembling the Case

2.4 POWER CONNECTION

2.4.1 CHECKING THE OPERATING VOLTAGE

Your Model 20B has been factory set to operate at the voltage marked on the label affixed to the bottom rear of the programmer. Check that the line voltage is the same as the voltage on the label before operating the programmer.

2.4.2 GROUNDING THE UNIT

The Model 20B's power cord contains 3 conductors. When the cord is connected to a 3-wire (grounded) AC power outlet, the ground connector grounds the unit, eliminating the possibility of shock. If a 3-wire power system is not available, a 3-to-2-wire adapter may be used, BUT THE GROUND LEAD OF THE ADAPTER MUST BE CONNECTED TO AN EARTH GROUND. Do not use any device (such as a 2-conductor extension cord) that would break contact between the unit and an earth ground.

WARNING

Failure to ground the unit may create a shock hazard.

2.5 SERIAL INTERFACE

2.5.1 ACCESSING

Status switches for parity, stop bits, and baud rates are mounted on the Serial I/O Board, part number 702-0066-001. Figure 2-2 shows a top view of these switches and how to set them.

2.5.2 CABLING

The Model 20B has an RS232C receptacle for connection to a host system. Figure 2-3 shows a scheme for interconnecting the programmer, computer, and/or a CRT. Table 2-2 describes the function of each connector pin of the RS232C receptacle, and Figure 2-4 shows suggested interconnection methods.

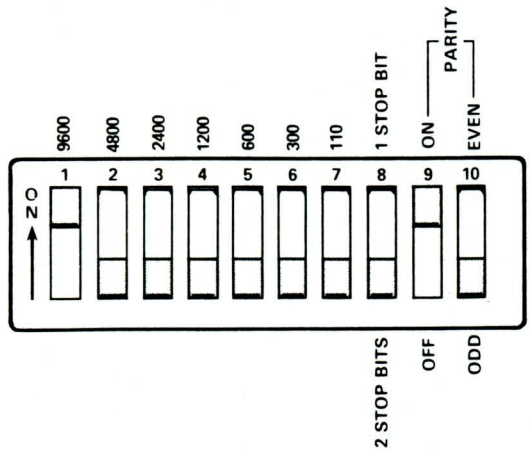


Figure 2-2. Serial I/O Selection Switches

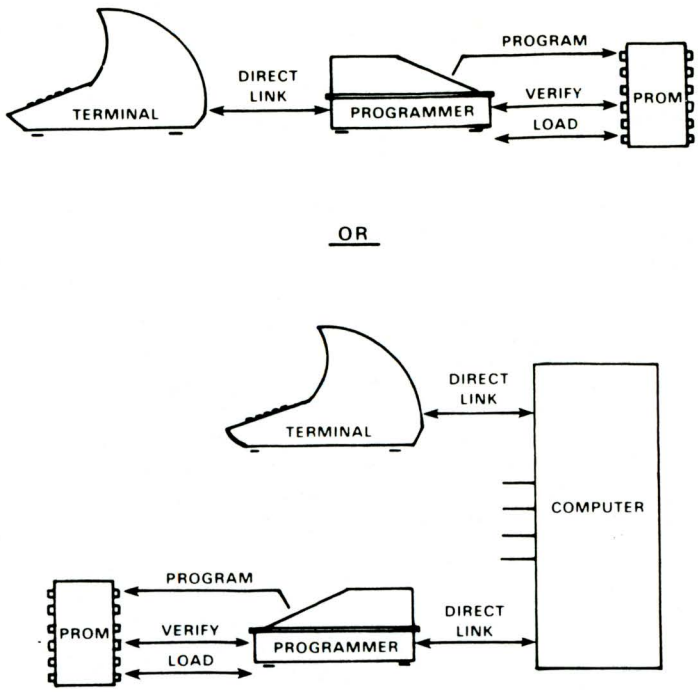
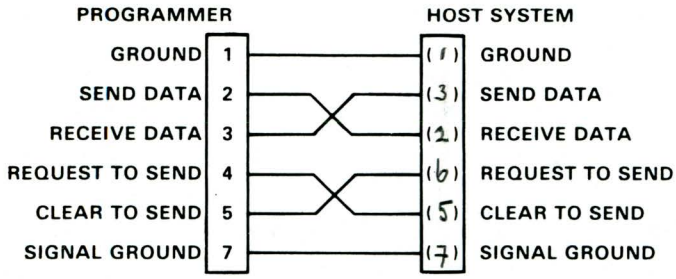


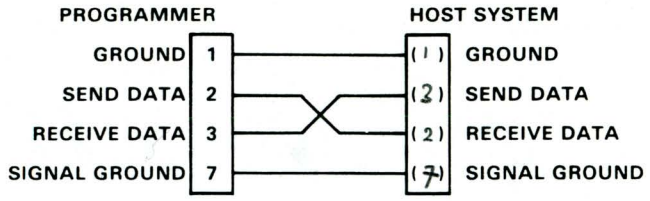
Figure 2-3. Programmer Installed for Remote Control

Table 2-2. Connector Pin Assignments

PIN NO.	SIGNAL	DESCRIPTION
1	Ground	In the RS232C environment this line is common for the −12 volt source and provides a safety ground connection to the RS232-compatible terminal.
2	Send Data	Transmits data using RS232C voltage levels (+12V and −5V)
3	Receive Data	Accepts data using RS232C voltage levels.
4	Request to Send	This line in normally held high by the programmer. It is dropped to inhibit data transmission from the peripheral.
5	Clear to Send	A high level on this line allows the programmer to send data. A low level inhibits data transmission.
6		Not used.
7	Signal Ground	This line provides a common signal connection to the RS232C data terminal.
8-25		Not used.



a)RS232 Connection, Half/Full Duplex, with Handshake[4]



b)RS232 Connection, Half/Full Duplex, w/o Handshake

NOTES:

1. All signals are named with respect to the originating unit.
2. All undesignated pins are to be left open.
3. For applications that do not require handshaking, the programmer's clear to send line is pulled up internally.
4. Required for the 1P Programming Mode. Consult paragraph 3.3.3.

Figure 2-4. Interconnection Methods

2.6 REPACKAGING FOR SHIPMENT

If you need to ship your Model 20B to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by model number, serial number and name.

If you use the original shipping container, place the instrument in the container with appropriate packing material and seal the container with strong tape. If you use another container, choose a heavy carton, wrapped with heavy paper or plastic. Use appropriate packing material and seal the carton well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

SECTION 3
OPERATION

3.1 OVERVIEW

Front panel operation of the Model 20B consists of three steps:

1. Key in the desired mode of operation,

2. Key in the type of device to be programmed, read or verified, and

3. Execute the operation

The Model 20B has 9 operating modes: Program, 1P, 2P, Verify, Read, Select, Format, Remote Control, and Diagnostic. The modes are explained in paragraph 3.2.2. All 24 and 28 pin EPROMs may be programmed in either the front panel programming modes (P, 1P, 2P) or the remote control mode (rc). All 40-pin devices (single chip microcomputers with EPROM) may only be programmed in remote control (rc) mode using an optional plug-in 40-pin socket adapter.

NOTE

The Diagnostic mode is not used in normal programmer operations. Instead, it is used periodically to check critical programming parameters and is therefore covered separately in Section 4.

In **remote control operation**, all instructions to the programmer are sent as single-character commands through the Model 20B's serial port. See section 3.5.

3.2 PREOPERATIONAL PROCEDURES

3.2.1 PRECAUTIONS

Before operating the Model 20B for the first time, check the set-up procedures in Section 2. Then note the following precautions:

DO NOT turn the main power switch on or off when a device is in either socket. Voltage transients at power-on or power-off can damage PROMs.

DO NOT insert or extract a device during programming. The "action symbol," a 2-digit number counting down, indicates that the PROM is being programmed.

DO NOT allow anything to obstruct airflow through the programmer's cooling vents. Doing so could overheat and damage sensitive components.

DO insert devices correctly in the socket. Pin 1 of the device must be on the left as you face the programmer; otherwise the PROM may be damaged. 24-pin devices must be inserted in the lower 24 pins of the 28-pin sockets. See Figure 3-1. The pin 1 indicators beside the socket are reminders that device pin 1 may be inserted only in socket pins 1 or 3.

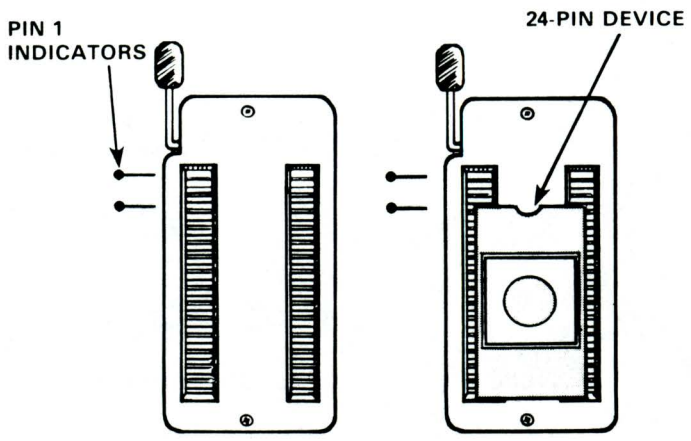


Figure 3-1. Correct Placement of PROMs in the Sockets

3.2.2 THE OPERATING MODES

Table 3-1 defines the Model 20B's 9 operating modes.

Table 3-1. Mode Descriptions and Mnemonics

MODE	DESCRIPTION	DISPLAY MNEMONIC
Program	Performs illegal-bit test and blank check, then programs data from master device into Copy-Socket device, then verifies data, bit by bit, between the devices.	P
1P	Inputs 2K-byte segment of data from a data source and then programs it into blank device. Automatically repeats this input-then-program sequence until entire PROM is programmed. Controls data source with RTS and CTS signals.	1P
2P	Inputs 2K-byte segment of data from a data source and then programs it into blank device. Automatically repeats this input-then-program sequence until entire PROM is programmed. Controls data source with X-ON and X-OFF signals.	2P
Verify	Compares data, bit by bit, between master device and Copy-Socket device; used to reverify already programmed devices.	CP
Read	Reads the data in the master device then computes and displays the sum-check.	rd
Select	Allows operator to instruct the programmer which device is installed in the socket(s) for a Program, Read, or Verify operation.	SEL
Format	Allows selection of Translation Format used in 1P, 2P and Remote Control modes.	For
Remote Control	Disables front panel controls and allows the programmer to be remotely controlled through its serial I/O port.	rC
Diagnostic	Each step in this mode turns on one voltage and applies it to one or more socket pins for measurement or trouble-shooting.	d

3.2.3 TURN-ON

a. Check the AC power label on the bottom rear of the programmer to be sure that the listed voltage matches the line voltage of the power source.

b. Remove any PROMs from the front panel sockets.

c. Turn the AC power switch on.

3.2.4 PROM SELECTION

In the Select mode, pressing the NEXT or LAST key steps forward or backward through the list of PROMs which the Model 20B programs. Table 1-1 gives the list of PROMs and PROM codes used by the Model 20B.

3.2.5 CHECK-OUT PROCEDURE

Before programming a PROM for the first time with the Model 20B, familiarize yourself with the key functions in Table 3-2.

Table 3-2. Key Functions

KEY	FUNCTIONS
NEXT	Steps forward through the modes.
	Steps forward through the devices in the Select mode.
	Steps forward through the formats in the Format mode.
	Steps forward through the steps in the Diagnostic mode.
	Inputs 2K-byte data segments in the 1P and 2P modes.
LAST	Steps backward through the modes.
	Steps backward through the devices in the Select mode.
	Steps backward through the formats in the Format mode.
	Steps backward through the steps in the Diagnostic mode.
START/STOP	Starts an operation in the chosen mode.
	Stops an operation in the chosen mode.

Now complete the check-out procedure in Table 3-3. Press the keys listed in the PRESS column; the DISPLAY column shows what should appear in the 4-character display for each step.

Table 3-3. Check-out Procedure

STEP	PRESS	DISPLAY SHOWS	DESCRIPTION
1	NEXT	PROM Code	Steps forward one device.
2	NEXT	PROM Code	Steps forward one device.
3	LAST	PROM Code	Steps backward one device.
4	LAST	PROM Code	Steps backward one device.
5	START/STOP	SEL	Locks in last device displayed and exits Select mode.
6	NEXT	rd	Steps forward one mode to Read mode.
7	NEXT	CP	Steps forward one mode to Verify mode.
8	NEXT	P	Steps forward one mode to Program mode.
9	NEXT	1P	Steps forward one mode to 1P mode.
10	NEXT	2P	Steps forward one mode to 2P mode.
11	LAST	1P	Steps backward one mode to 1P mode.
12	NEXT	2P	Steps forward one mode to 2P mode.
13	NEXT	For	Steps forward one mode to format mode.
14	START/STOP	F83	Enters format mode.
15	NEXT	F10	Steps forward one format.
16	NEXT	F50	Steps forward one format.
17	NEXT	F81	Steps forward one format.
18	NEXT	F82	Steps forward one format.
19	NEXT	F86	Steps forward one format.
20	START/STOP	For	Locks in last format and exits Format mode.
21	NEXT	RC	Steps forward one mode to Remote Control mode.
22	NEXT	d	Steps forward one mode to Diagnostic mode.
23	START/STOP	d 01	Locks in Diagnostic mode.
24	NEXT	d 02	Steps forward one step in Diagnostic mode every time key is pressed.
	NEXT	d 03	
	NEXT	d 04	
25	LAST	d 03	Steps backward one step in Diagnostic mode every time key is pressed.
	NEXT	d 04	
26	START/STOP	d	Stops operations and exits the Diagnostic mode.
27	NEXT	SEL	Steps forward one mode to Select mode.

3.3 USING THE MODES

Paragraphs 3.3.1 through 3.3.6 explain how to use the Select, Program, Verify, 1P, 2P, Read, and Format modes. Paragraph 3.5 explains the Remote Control mode.

3.3.1 THE SELECT MODE

In the Select mode use the NEXT key or LAST key to step through and display the devices.

a. Turn the power switch on. The programmer will power up in the Select mode and display *2708*.

b. Press the NEXT key to step forward through the list of devices,

or

Press the LAST key to step backward through the list of devices.

c. When the desired PROM code appears in the display, press the START/STOP key. The Model 20B is now prepared to read, program or verify the chosen device.

NOTE

Although 40-pin devices may be selected from front panel operation, programming can only take place in the remote control mode.

3.3.2 THE PROGRAM MODE

To program 24- or 28-pin MOS PROMs, refer to the instructions that follow. To program a 40-pin device, consult paragraph 3.5.

a. Use the Select mode to select the device you wish to program.

b. Press the NEXT key repeatedly until *P* appears in the display.

c. Insert your master device in the Master Socket and a blank device of the same type in the Copy Socket.

d. Press the START/STOP key.

The Model 20B first makes an illegal-bit check of the device in the Copy Socket. If an illegal bit occurs, the display will alternate between *P=C* and *Er 21*, and the Model 20B will abort the operation.

If there are no illegal bits, the programmer performs a blank check. If the device is not blank, the display will alternate between *P=C* and *Er 20*. If you wish to program the device anyway, press the START/STOP key again.

Next, the Model 20B programs the PROM. After the device is programmed, the Model 20B executes an automatic verify routine which automatically compares every bit in one PROM with the corresponding bit in the other PROM.

After the automatic verify is done, if the devices verify, the display will alternate between *P=C* and a 4-digit sum-check. If the devices do not verify, the display will alternate between *P=C* and *ER 23*.

3.3.3 THE 1P AND 2P MODES (For Programming Devices without a Master Device)

General Description. The 1P and 2P modes make programming easier when programming data must be input to RAM through the serial port.

NOTE

When no master device is available, a blank device can be programmed in the 1P, 2P, or Remote Control mode. After programming one device, you can program duplicates most easily in the Program mode.

In the 1P and 2P modes, the Model 20B instructs the transmitting instrument to output 2K bytes of data; the Model 20B stores this data in RAM. You may program your blank device with this data or input 2K segments of data to RAM, one at a time, until you find the data you wish to program into the first 2K segment of the blank device. Then press START/STOP and the Model 20B automatically inputs and programs consecutive 2K segments of the source data until the entire device is programmed.

Typical Uses. There are 2 typical uses of the 1P and 2P modes.

1. Locating and programming data from a large data file. EXAMPLE: You have a data file with addresses Ø through 32K, and you wish to program a 2K-byte device from data between addresses 16K and 18K. You can read through the data file up to the starting address, 16K, and then program the device with the desired data.

2. One-step programming of devices larger than 2K bytes when no master device is available. EXAMPLE: You have a data file from which to program an 8K-byte device. The 1P or 2P mode allows you to automatically input and program four 2K data segments from your file, all in one step.

The 1P Mode. In the 1P mode the Model 20B controls the transmitting instrument via the RTS and CTS handshake signals. See Figure 2-4 for required cabling.

The 2P Mode. In the 2P mode the Model 20B sends ASCII X-ON and X-OFF characters to control the sending instrument. The sending instrument must be able to respond to these signals.

Device Boundaries. The Model 20B computes a device boundary. This is done after pressing the START/STOP key, but before the first incoming data byte is stored to

RAM. The Model 20B device boundary is described by the expression

N • word limit of selected device

where N is a positive whole number, or zero. (For example, the device boundaries for a 4K device are 0, 4K, 8K, 12K, 16K, etc. up to 60K. These boundaries are displayed in hexadecimal notation as 0, 1000, 2000, 3000, 4000, etc. up to F000.)

The Model 20B will then store the incoming data to RAM and select the appropriate 2K segment of the device. This selection is based on the incoming data's address relative to RAM word zero. RAM word zero represents the computed device boundary.

To program the device with the data in RAM, press START/STOP again. The Model 20B programs this segment and then alternately inputs and programs consecutive 2K segments automatically until the device is programmed.

On the other hand, you can press NEXT instead of START/STOP in order to input another 2K segment of data starting with the *first address equal to or above the next higher device boundary.* The Model 20B will display the incoming address fields, but it will not store the incoming data to RAM until the incoming data address is equal to or above the new higher device boundary. After this incoming data has filled the 2K RAM, the Model 20B displays that device boundary, alternating with the mode. You can repeat this process by pressing NEXT until the desired 2K data segment is in RAM. As soon as you press START/STOP, the Model 20B programs this segment and then alternately inputs and programs consecutive 2K segments automatically until all segments of the device are programmed.

Programming. To program devices in the 1P or 2P mode:

a. Connect the programmer to the source of programming data, according to Section 2. Be sure the connection allows bidirectional handshake signals. (1P Mode = RTS + CTS, 2P = X-ON, X-OFF)

b. Use the Select mode to select the device you wish to program.

c. Use the Format mode to select a translation format. The exception to this is the Binary (10) and ASCII-Hex Space (50) formats. The 1P and 2P modes will not accept data expressed in these translation formats.

d. Insert a blank device in the Copy socket.

e. Press the NEXT key repeatedly until "1P" or "2P" appears on the display.

f. If the sending instrument has a timeout routine, disable it.

NOTE

On input to the programmer, any addresses in the data stream will appear on the display.

g. Initiate an output operation from the sending instrument in the following order:

   1. In the 1P mode, press START/STOP on the 20B first, then initiate the sending instrument;

   2. In the 2P mode, initiate an output operation from the sending instrument first, then press START/STOP on the 20B. This will allow data to be received from the remote source.

h. The Model 20B will

   1. Perform a blank test. If the device in the Copy Socket is non-blank, operation will not continue.

   2. Compute a device boundary based on the device size and the first incoming address.

   3. Store the first 2K data segment in RAM.

   4. Halt the sending instrument and display the computed device boundary alternating with the mode.

i. If the desired device boundary is displayed, go to step l. If not, go to step j.

j. Press NEXT. The Model 20B

   1. Computes the next higher device boundary.

   2. Inputs data, storing the first byte that has an address equal to or above the device boundary into RAM.

   3. Halts the sending instrument and displays the device boundary alternating with the mode.

   4. Every time NEXT is pressed, repeats steps 1—3.

k. When the desired device boundary appears, go to step l. Until it appears, repeat step j.

l. Press START/STOP. The Model 20B

   1. Programs RAM data into the first 2K segment of the device and then verifies RAM data with device data. If they are not identical, the programmer signals an error.

   2. Inputs the next 2K segment of data into RAM.

   3. Halts the sending instrument.

   4. Programs RAM data into the next 2K segment of the device and then verifies RAM data with device data. If they are not identical, the programmer signals an error.

   5. Repeats steps 2—4 until the device is programmed.

   6. Displays the sum-check of the programmed data.

3.3.4 THE VERIFY MODE

To verify a 40-pin device, consult paragraph 3.5.

Use the Verify mode to verify already programmed PROMs.

a. Enter the Select mode to select the device you wish to verify.

b. Press the NEXT key repeatedly until "CP" appears in the display.

c. Insert the two devices to be compared in the two sockets.

d. Press the START/STOP key.

The Model 20B will compare every bit in one device with the corresponding bit in the other device. If this verification is completed successfully, the display will alternate between *CP=C* and a 4-digit sum-check. If the devices do not verify, the display will alternate between *CP=C* and *ER 23*.

3.3.5 THE READ MODE

In the Read mode, the Model 20B reads the data from the PROM in the Master Socket and then calculates and displays the sum-check. To read a 40-pin device, refer to paragraph 3.5.

a. Use the Select mode to select the device you wish to read.

b. Press the NEXT key repeatedly until "rd" appears in the display.

c. Insert the device to be read in the Master Socket.

d. Press the START/STOP key.

The Model 20B will read the data in the device and then display the sum-check of the data.

3.3.6 THE FORMAT MODE

The format mode is used to step through and display or select the desired translation format. If a specific format is not selected, the default is Intel Intellec 8/MDS (83) format.

a. Press the NEXT key repeatedly until "For" appears in the display.

b. Press the START/STOP key. A Format code will appear. Refer to the formats that follow and Appendix A.

c. Press the NEXT key until the desired Format code appears.

or

Press the LAST key to step backward through the list of formats until the appropriate Format code is displayed.

d. When the desired Format code appears in the display, press the START/STOP key. This will lock in your Format code selection.

When transferring data to and from the Model 20B, use one of the following data translation formats:

- Binary Transfer - 10
- ASCII Hex Space - 50
- MOS Technology - 81
- Motorola Exorciser - 82
- Intel Intellec 8/MDS - 83
- Tektronix Hexadecimal - 86

These formats are discussed in greater detail in Appendix A.

3.4 ERRORS AND WHAT TO DO ABOUT THEM

Error-checking routines are part of each Model 20B mode. Table 3-5, at the end of this section, gives a complete list of error codes and the action to take if they occur.

3.5 REMOTE OPERATION

The following paragraphs describe entering and exiting remote control and the command set available for data transfer and programming. Remote control commands can be sent from a terminal, or written into a controlling computer's operating software, allowing it to control the Model 20B as it would any peripheral. Commands are then generated by the computer according to its software or in response to keyboard entries made by an operator. The computer sends these commands to the programmer, which executes the command and then sends an appropriate response back to the computer.

Remote control operation also allows the operator to program 40-pin single chip microprocessors. The 40-pin devices require use of an optional plug-in socket adapter. The 40-pin devices cannot be programmed, read or verified in front panel operation. This is because front panel operation uses master and copy sockets.

Remote control commands are grouped as follows:

- Control commands (see paragraph 3.5.2) are used to execute or suspend a command.
- Utility commands (see paragraph 3.5.3) tell the programmer to retrieve information or access memory locations within RAM.
- Device commands (see paragraph 3.5.4) read, program, verify and identify devices.
- I/O commands (see paragraph 3.5.5) set parameters for I/O transfers and send data to or from a peripheral computer.
- Edit commands (see paragraph 3.5.6) manipulate data within programmer RAM only.

Paragraph 3.5.8 describes the programmer's responses.

3.5.1 ENTERING REMOTE CONTROL

To enter remote control, use the following procedure:

a. Power up all systems.

b. On the programmer press the START/STOP switch.

c. Press the NEXT or LAST switch until *rC* appears on the programmer display.

d. Press the START/STOP switch. The programmer's keyboard will remain inoperative until control is returned to the programmer.

3.5.2 CONTROL COMMANDS

RETURN

1. RETURN executes each command. It must be sent to the programmer immediately after the command. All commands except Edit mode commands are ignored if not followed by RETURN.

2. Exits the Edit mode.

ESC
BREAK

The ESCAPE and BREAK commands cause the programmer to unconditionally halt (abort) any operation in progress, output the prompt character (>) and await further instruction from the host system.

3.5.3 UTILITY COMMANDS

SOFTWARE CONFIGURATION NUMBER — **G** RETURN

On this command the programmer sends the 4-digit hex number representing the software revision of the programmer.

SUM-CHECK — **S** RETURN

Instructs the programmer to calculate the sum-check of RAM data from the begin RAM address to the word limit of the selected device (up to 2K), or blocksize, whichever is smaller; and to output the sum-check to the computer. Section 8 describes the sum-check.

ERROR CODE INQUIRY — **X** RETURN

Instructs the programmer to output the error codes accumulated in scratch pad memory and then to clear the memory. Up to 8 error codes can be stored. See Table 3-5 for a complete list of error codes.

SET BLOCK SIZE — HHH **;** RETURN

This command specifies the highest RAM address (HHH-1) affected in the following commands: Insert (I), Delete (X), Fill (Y) and List (Q). It also specifies the number of data bytes for Blank Check (B), Illegal Bit Test (T), Load (L), Program (P) and Verify (V) operations. The default value is the size of RAM or the chosen device, whichever is smaller.

SET BEGIN DEVICE — HHHH **:** RETURN

Sets a 4-digit hex address (HHHH) telling the programmer the first device address to use for programming, verifying, blank checking, illegal bit testing and loading of device data. Default value is **Ø**. If the beginning device address is greater than **Ø**, addresses beyond 2K (or device word limit) will wrap around to device word **Ø**. Block size remains unchanged.

verderdan

SET BEGIN RAM — HHHH **<** RETURN

This command, preceded by a 4-digit hex address, sets the first RAM address to be used for data transfers. Default Value — **Ø**.

LIST MEMORY — HHHH **#** RETURN

Instructs the programmer to output the contents of RAM memory to the host system, beginning at the specified 4-digit hex address (HHHH)

OPEN MEMORY LOCATION — HHHH **$** RETURN

Instructs the programmer to examine the location specified by the 4-digit hex address (HHHH) and output the address and its data to the host system. The specified address must be less than the address given in the Set Block Size (;) command. After receiving this command, the only commands that the programmer will recognize are Edit mode commands; see Section 3.5.6.

EXIT REMOTE CONTROL — **Z** RETURN

Returns control of the programmer to the programmer's front panel. All operating parameters and RAM data are retained. Programmer display shows *rC = C*.

3.5.4 DEVICE COMMANDS

ILLEGAL-BIT TEST — **T** RETURN

Instructs the programmer to test the device for illegal bits. An illegal bit is a programmed bit in the device that does not exist in RAM. (See Section 8.) A prompt character (>) is returned following a successful test. A fail character (F) indicates detection of an illegal bit.

BLANK CHECK **B** RETURN

Instructs the programmer to search the device for programmed bits. (See Section 8.) The return of a prompt character (>) indicates a blank device; a fail character (F) indicates a nonblank device.

SELECT FAMILY AND PINOUT FFPP **@** RETURN

A 2-digit Family Code (FF) and a 2-digit Pinout Code (PP) are sent to the programmer ahead of this command. The Family and Pinout Codes are shown in Table 1-1. These codes identify the particular device to be used for device operations.

PROM CODE INQUIRY **[** RETURN

The programmer outputs a 4-digit hex number consisting of a 2-digit Family Code and a 2-digit Pinout Code. The Family and Pinout Codes are shown in Table 1-1. These codes identify the particular device to be used for device operations.

RESPOND **R** RETURN

This command instructs the programmer to indicate the status of the device selected by outputting data in the form AAA/B/C or AAAA/B/C to the computer, where A, B and C represent hexadecimal characters. AAA = word limit of 4K or smaller devices; AAAA = word limit of devices larger than 4K; B = word size, 8 bit only; C = VOH or VOL — 0 for VOH, 1 for VOL.

LOAD **L** RETURN

Instructs the programmer to load data into RAM from the device in the Copy Socket. A prompt character (>) indicates a successful load operation; a fail character (F) indicates that the device data did not load.

PROGRAM **P** RETURN

Instructs the programmer to program RAM contents into the device in the Copy Socket. A prompt character (>) indicates a successful programming operation; a fail character (F) indicates failure to program.

VERIFY **V** RETURN

Instructs the programmer to compare RAM data with the data of the device in the Copy Socket. A prompt character (>) indicates that the device and RAM are identical; a fail character (F) indicates that they are not identical.

3.5.5 I/O COMMANDS

SELECT TRANSLATION FORMAT FC **A** RETURN

This command selects the input or output data translation format expressed by the format code (FC) in the command. Paragraph 3.3.6 lists the format codes. Default Value = Intel Intellec 8/MDS Format, Select Code 83.

NOTE

All translation formats are detailed in Appendix A.

INPUT DATA **I** RETURN

Instructs the programmer to accept data in the selected format through the serial port. Any error on input returns the fail character (F). Successful input returns the prompt character (>).

NOTE

On input, any addresses in the data stream will appear on the display.

OUTPUT DATA **O** RETURN

Instructs the programmer to format RAM data in the selected format and output it to the serial port. Successful output is indicated by a prompt character (>). Any error will return the fail character (F).

COMPARE DATA **C** RETURN

Instructs the programmer to compare data in RAM with data from the serial port. Identity of the two returns the prompt character (>). Nonidentity is indicated by the fail character (F).

SET RECORD SIZE HH **M** RETURN

The 2 hex characters (HH) before M indicate the number of data bytes per record for the O and # commands. Default value is 16 bytes per record.

SET NULLS HH **U** RETURN

The 2 hex characters (HH) before U set the number of nulls that follow carriage returns and line feeds in serial output operations. Default value is Ø. (Enter FF before U to obtain no nulls and no line feed following the carriage return.)

SET ADDRESS OFFSET HHHH **W** RETURN

The 4 hex characters (HHHH) before W specify an address that is subtracted from all addresses input to the programmer and added to all addresses output from the programmer. Default value is Ø.

EXIT EDIT MODE RETURN

Disallows the programmer from executing Edit mode commands until it receives another OPEN MEMORY LOCATION command. See section 3.5.3.

3.5.6 EDIT MODE COMMANDS

The Edit mode commands are accessible only after an OPEN MEMORY LOCATION command has been sent to the programmer.

NOTE

In the Edit mode the RETURN key does ***not*** *execute commands; rather, it causes the programmer to exit the Edit mode. See section 3.5.5.*

WRITE DATA AND DISPLAY NEXT ADDRESS HH **SPACE**

This command stores data (HH) at the current RAM address, then outputs the next address and its data to the host system. Sending a Space character without HH outputs the next address and its data without altering any data.

WRITE DATA AND DISPLAY PREVIOUS ADDRESS HH /

This command stores data (HH) at the current RAM address, then outputs the previous address and its data to the host system. Sending a / character without HH displays the previous address and its data without altering any data.

INSERT DATA HH I

This command stores data (HH) at the current RAM address and shifts all data at higher addresses up one address. The amount of data affected can be limited by the Set Block Size command (;). The data at the highest *affected* RAM address is lost.

DELETE DATA X

This command deletes the data at the current RAM address and shifts all data at higher addresses down one address. The amount of data affected can be limited by the Set Block Size command (;). The highest *affected* RAM address is filled with zeros.

FILL MEMORY HH **Y**

This command enters data (HH) in all memory locations beginning with the current address and ending with the address specified in the Set Block Size command (;).

3.5.7 RESPONSE CHARACTERS

The programmer must send a response character — a prompt (>), F, ?, or E — to the host system before it can execute another command (except a control command). Table 3-4 shows how to interpret each response character.

Table 3-4. Response Characters

THE PROGRAMMER OUTPUTS:	
THIS RESPONSE:	**IN THESE CASES**
>	1. on entering remote control 2. after successfully executing a command 3. after the BREAK or ESCAPE key has halted a command.
F	after failing to execute a valid command
?	after receiving an invalid command or a message it did not "understand"
E	when a PROM is not installed correctly or the incorrect PROM code was selected.

Table 3-5. Error Codes

ERROR CODE	ERROR	REMEDY
Er 20	Nonblank PROM	Remove PROM, or press START/STOP to continue programming if desired.
Er 21	Illegal bit in PROM	Remove PROM; it cannot be programmed to desired bit pattern.
Er 23	PROM does not verify with source data	Remove PROM and do not use it because it may be defective.
Er 27	Device address too high	Enter correct address.
Er 29	Non-compare	Reload RAM. If error recurs, check programmer's Port and transmitting instrument's Port. Also, check for nonsequential addresses in source data.
Er 31	Upside-down PROM	Place PROM right side up.
	Shorted PROM	Remove PROM and do not use it.
Er 32	Misjustified or upside-down PROM	Place PROM right side up in lower 24 socket contacts.
Er 34	Incorrect Family and Pinout Code	Enter correct Family and Pinout code.
Er 35	Data register failed on power-up	Turn power off and see Section 6, Troubleshooting.
Er 36	Data block too small	Semicolon (;) command must be 10 (hex) or greater when programming 3V devices. Smaller block sizes could damage the PROMs during programming.
Er 37	Improper Operation	Device must be operated in remote control.
Er 38	Voltage error	PROM in Master or Copy Socket may be faulty. Replace with known-good PROMs and repeat operation. If error recurs, turn power off and see Section 6, Troubleshooting.
Er 48	Serial port buffer overrun	Check handshake lines for proper connection. Also, check the baud rate.
Er 63	RAM write error	RAM chip may be faulty. Replace with known-good chip.
Er 65	Program memory failure	Turn power off and see Section 6, Troubleshooting.
Er 66	Unknown interrupt	Continue operation. If error recurs, see Section 6, Troubleshooting.
Er 67	Non-hex character	Incorrect entry. Reenter hex data correctly.
Er 70	Power-on failure	Turn power off and see Section 6, Troubleshooting.
Er 81	Parity error	Check setting of parity switches on Serial I/O Board.
Er 82	Sum-check error	Check incoming data.
Er 84	Non-hex character on serial input	Check incoming data.
Er 91	Non-hex character in address	Check incoming data.
Er 93	Record count error	Check incoming data.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibrate the Model 20B every three months, or more often if programming yields are low or the operating environment is dusty or excessively humid.

Calibration consists of three parts:

1. **Power supply measurements.** These are measurements of the DC supply voltages. All other voltages depend on these supplies; therefore, this part must be done first.

2. **DC Calibration.** This part consists of measuring and adjusting other critical DC voltage levels.

3. **Waveform Observation.** This part consists of observing programming waveforms for compliance with the device manufacturers' critical voltage and timing specifications.

Figure 4-2 is an operator's flowchart of the calibration procedure, with references to the section in text where each part is covered.

NOTE

For calibration, remove PROMs from both sockets, unless otherwise specified.

4.2 THE MEASUREMENT CHART

The Measurement Chart contains the information necessary for all DC calibration tests.

The Measurement Chart presents calibration information as follows:

- The STEP NO. column tells which step to use for each test. Step numbers are set at the programmer keyboard.
- The TEST NO. column identifies individual tests.
- The TEST DESCRIPTION column identifies the functions being tested.
- The TEST LOCATION column tells which pins on the socket to probe for measuring voltages.
- The VOLTAGE columns specify allowable voltage ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the Model 20B until the problem is corrected.
- The ADJUSTMENT LOCATION column tells which potentiometer to adjust if a voltage is out of range.
- The COMMENTS column gives special instructions for particular tests.

4.3 MAKING DC VOLTAGE MEASUREMENTS

Voltage readings are made at the device sockets. Figure 4-1 shows the pin numbers for the sockets.

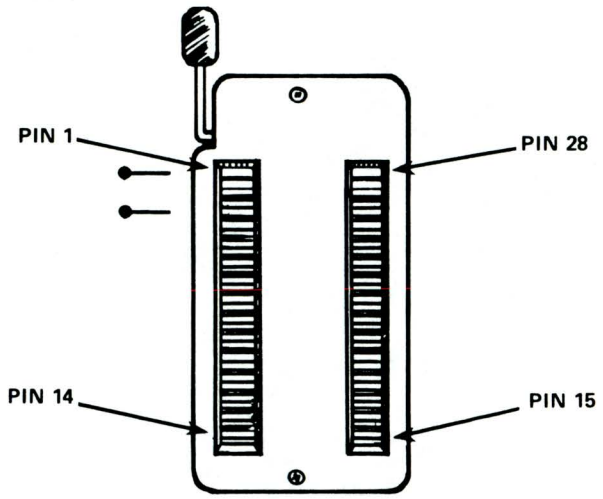


Figure 4-1. Pin Numbers of the Device Sockets

Connect the digital voltmeter as follows:

a. Connect the common lead of the DVM to ground, which is pin 14 on both sockets.

b. With the positive lead, probe the test points indicated on the Measurement Chart.

4.4 PERFORMANCE CHECK

4.4.1 DEFINITION

A performance check is a check of the programmer's DC voltage levels. Making a performance check does not calibrate the programmer, but it is an easy procedure for verifying that DC voltage levels are within tolerance. See the flowchart in Figure 4-3.

CAUTION

A performance check is not a substitute for calibration. If any DC voltage is out of range, calibrate the programmer before using it. See Section 4.5.

4.4.2 REQUIRED EQUIPMENT

To make a performance check you will need a digital voltmeter (Fluke 8000A or equivalent).

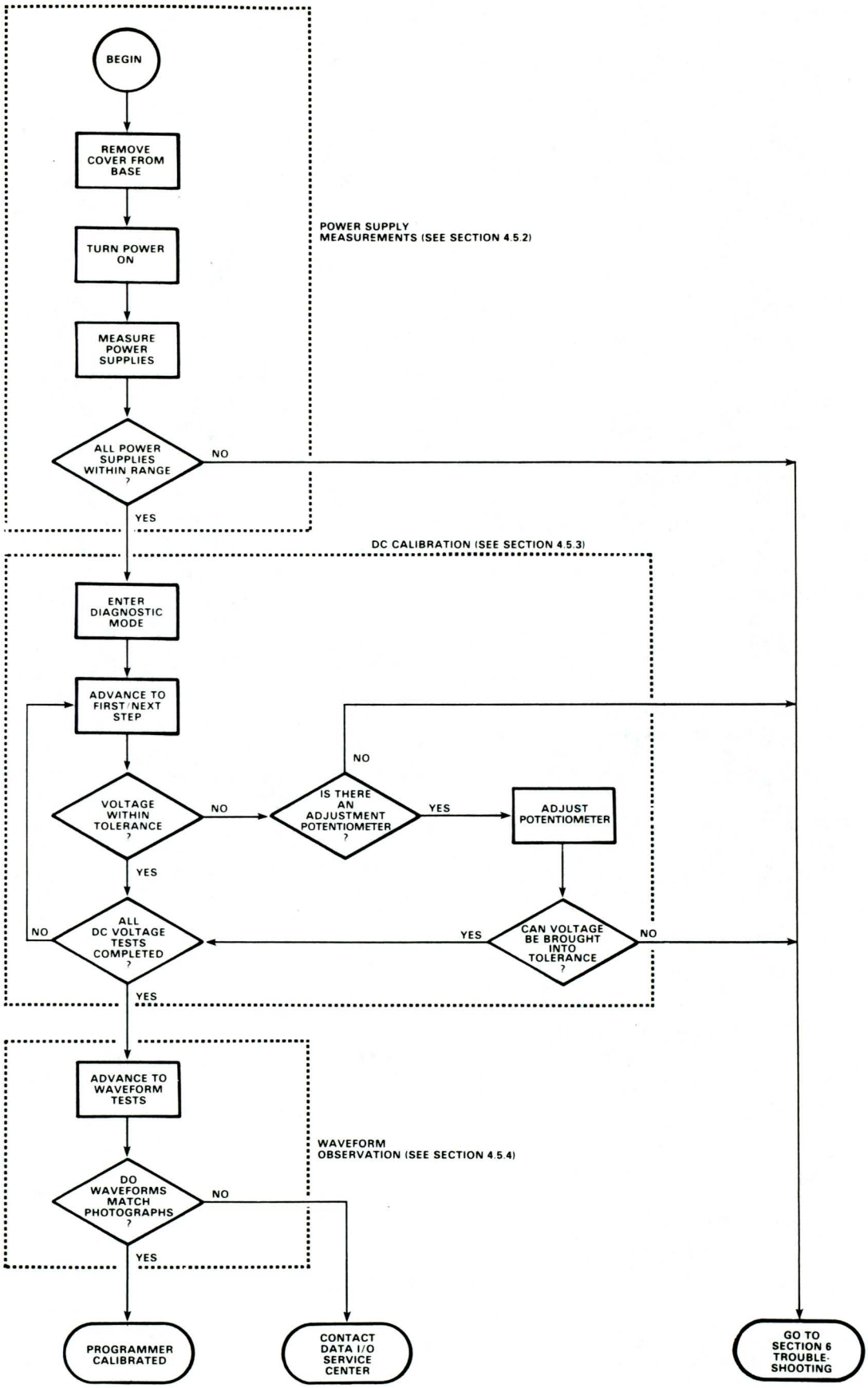


Figure 4-2. Operator's Flowchart for Calibration

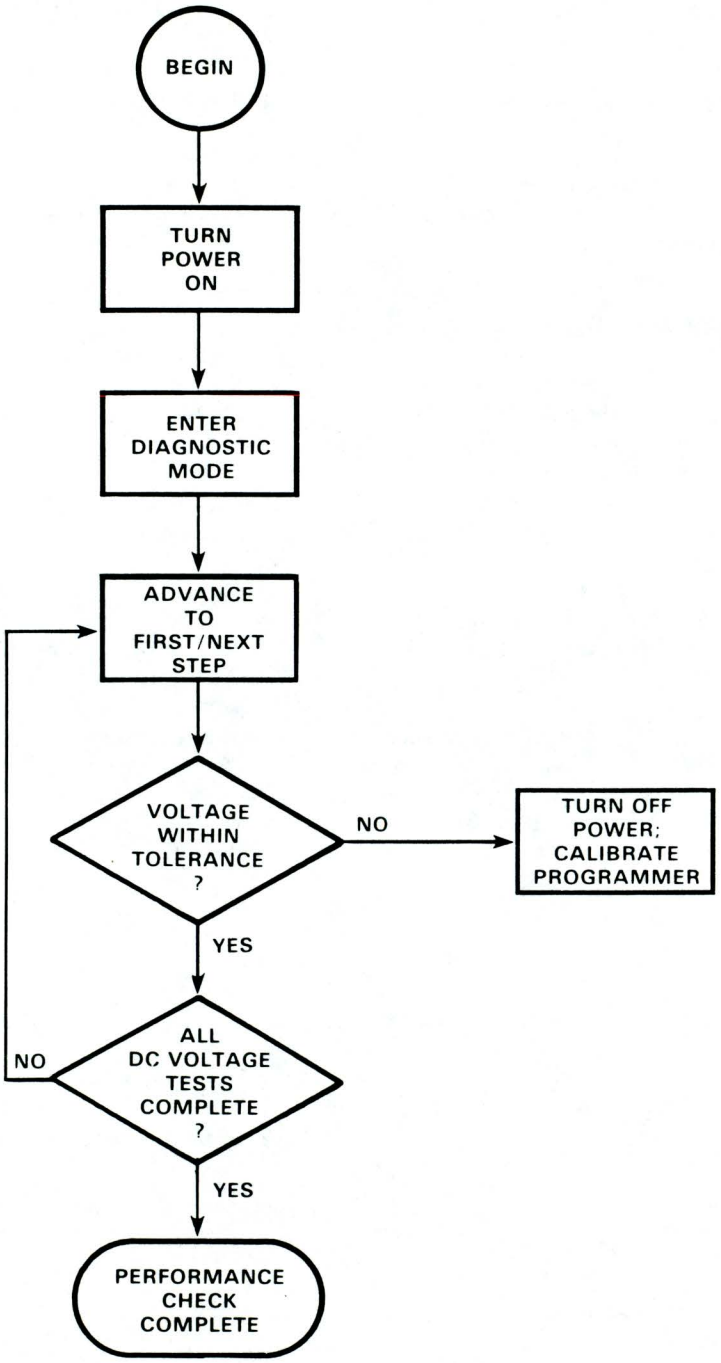


Figure 4-3. Operator's Flowchart for a Performance Check

4.4.3 ENTERING THE DIAGNOSTIC MODE

a. Turn the power switch on. The Model 20B will power up in the Select mode and the display will read 2708.

b. Press the START/STOP key. The programmer will leave the Select mode.

c. Press the NEXT key repeatedly until the display shows *d*.

d. Press the START/STOP key to lock in the Diagnostic mode. The display will show *d 01*, which refers to step 1 on the Measurement Chart.

4.4.4 MAKING THE PERFORMANCE CHECK

To make a performance check, select the appropriate Measurement Chart. For a performance check of the 28 pin socket, use Measurement Chart 017-0010-001. To check performance of the 40-pin socket adapter, use the Measurement Chart that is provided in the Socket Adapter Manual.

a. For step 1, measure the voltage at the point(s) specified in the TEST LOCATION column of the Measurement Chart. Note whether the measured voltage falls within the range.

b. For all succeeding steps, first press the NEXT key until the desired step number appears in the display, and then proceed as in step a, noting any voltage falling outside the given range. To return to a previous step, press the LAST key until that step number appears in the display.

c. If any voltage falls outside the specified range, calibrate the programmer as explained in paragraph 4.5.

4.5 CALIBRATION

4.5.1 REQUIRED EQUIPMENT

In order to calibrate the Model 20B, the following equipment is required:

- Digital voltmeter (Fluke 8000A or equivalent)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)
- Potentiometer-adjustment tool ("tweaker") or a small, flat-bladed screwdriver (blade less than ¼ inch wide)

4.5.2 POWER SUPPLY MEASUREMENTS

The first step in a complete calibration is to measure the Model 20B's power supplies.

a. Remove the cover of the programmer according to the procedure in section 2.2.

b. Turn the AC power switch on.

c. See Figure 4-4. Locate connector J2 on the Power Supply Card (part number 702-0072-001.) Pin 1 of J2 is identified by the white dot on the card; the white dot is next to the connector. Measurements must be made while the cable connected to J2 is in place.

d. Measure the power supplies according to Table 4-1. The table shows where to measure each power supply as

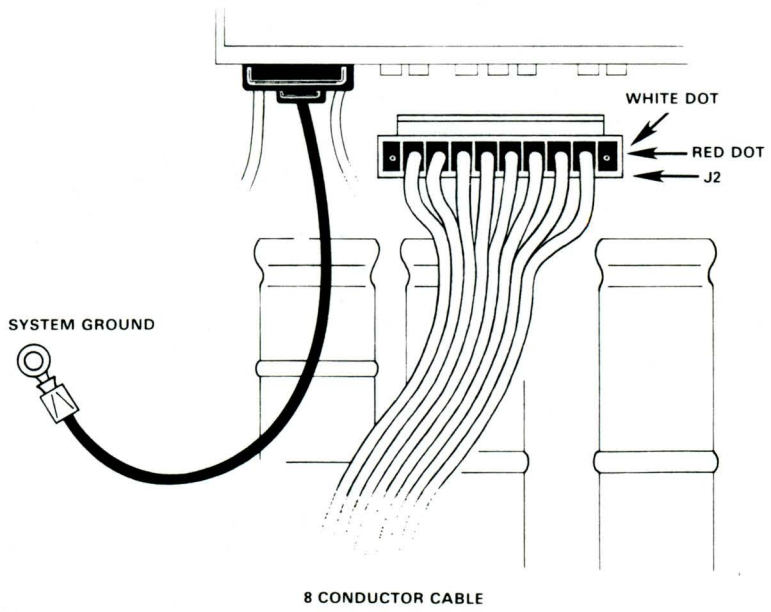


Figure 4-4. Locations for Power Supply Measurements

Table 4-1. Power Supply Voltages

SUPPLY	VOLTAGE RANGE MIN.	NOM.	MAX.	TEST LOCATION ON J2
+38 V	34.0	38.0	48.0	Pin 1
Gnd. Sense	−0.4	0.0	0.4	Pin 2
+5 V	4.75	5.00	5.25	Pin 3
+12 V	11.4	12.0	12.6	Pin 4
−14 V	−15.5	−14.0	−9.0	Pin 5
Gnd.	−0.4	0.0	0.4	Pin 6
−5 V	−5.25	−5.00	−4.75	Pin 7
+19 V	16.0	19.0	24.0	Pin 8

NOTES:

1. All test locations are on J2 on Power Supply Card, part number 702-0072-001. Place negative lead of DVM on system ground.
2. All circuit cards and cables must be installed.

well as the acceptable voltage range for each supply. To make the measurements, connect the negative lead to the system ground (see Figure 4-4). Then, place the positive lead of the DVM on the cable connectors going in to J2.

e. If a voltage is out of tolerance, go to Section 6, Troubleshooting. No adjustment of the power supplies is possible.

f. After completing all DC voltage tests on the Measurement Chart, observe programming waveforms according to the procedure in section 4.5.4. If any DC voltages are still out of range, consult Section 6, Troubleshooting.

4.5.3 DC CALIBRATION

If DC Calibration is required for the 40-pin socket adapter, use the Measurement Chart which is located in the appropriate socket adapter manual. DC Calibration for the 40-pin socket adapter is performed once calibration has been completed on the 28-pin socket. To calibrate the 28-pin socket, use Measurement Chart number 017-0010-001.

a. Refer to Figure 4-5, which shows the potentiometers used for voltage adjustments. These potentiometers are called out in the ADJUSTMENT LOCATION column of the Measurement Chart.

b. Advance to the Diagnostic mode. The display should show *d*.

c. Press the START/STOP key to lock in the Diagnostic mode. The display will show *d 01*, which refers to step 1 on the Measurement Chart.

d. For step 1 on the Measurement Chart, measure the voltage at the points specified in the TEST LOCATION column. If the voltage is out of range, bring it into range by adjusting the potentiometer called out in the ADJUSTMENT LOCATION column. Note if the voltage cannot be adjusted to within range.

e. For all succeeding steps, first press the NEXT key until the desired step number appears in the display, and then proceed as in step d. Note any voltages which fall outside the given range and adjust the voltage if an adjustment pot is called out in the ADJUSTMENT LOCATION column. To return to any previous step, press the LAST key until that step number appears in the display.

f. After completing all DC voltage tests on the Measurement Chart, observe programming waveforms according to the procedure in section 4.5.4. If any DC voltages are still out of range, consult Section 6, Troubleshooting.

4.5.4 WAVEFORM OBSERVATION

You can observe programming waveforms with an oscilloscope and compare them with the waveform photographs on the Timing Diagrams. If the programmer is calibrated, actual programming waveforms should match those in the photographs. If the waveforms do not match, contact your local data I/O Service Center.

Because the Model 20B generates a large number of waveforms, Data I/O recommends observing only the waveforms for the PROMs which you program.

Device Groups

The devices programmed by the Model 20B are divided into 2 groups for calibration purposes. Group 1 consists of single-pulse algorithm parts; group 2 consists of looping-address and variable-pulse algorithm parts (see Table 4-2).

For group 1 devices, critical waveforms can always be observed at the Copy Socket when the programmer is in the Diagnostic mode.

For group 2 devices, a preprogrammed master device must be installed in the Master Socket so that data line transitions can be observed at the Copy Socket. The preprogrammed master device should contain as many programmed bits as possible. This will produce the maximum number of waveshapes for observation on your oscilloscope.

The Timing Diagrams

This manual contains a timing diagram for each PROM family. Each timing diagram contains a set of waveform photographs that show critical programming parameters.

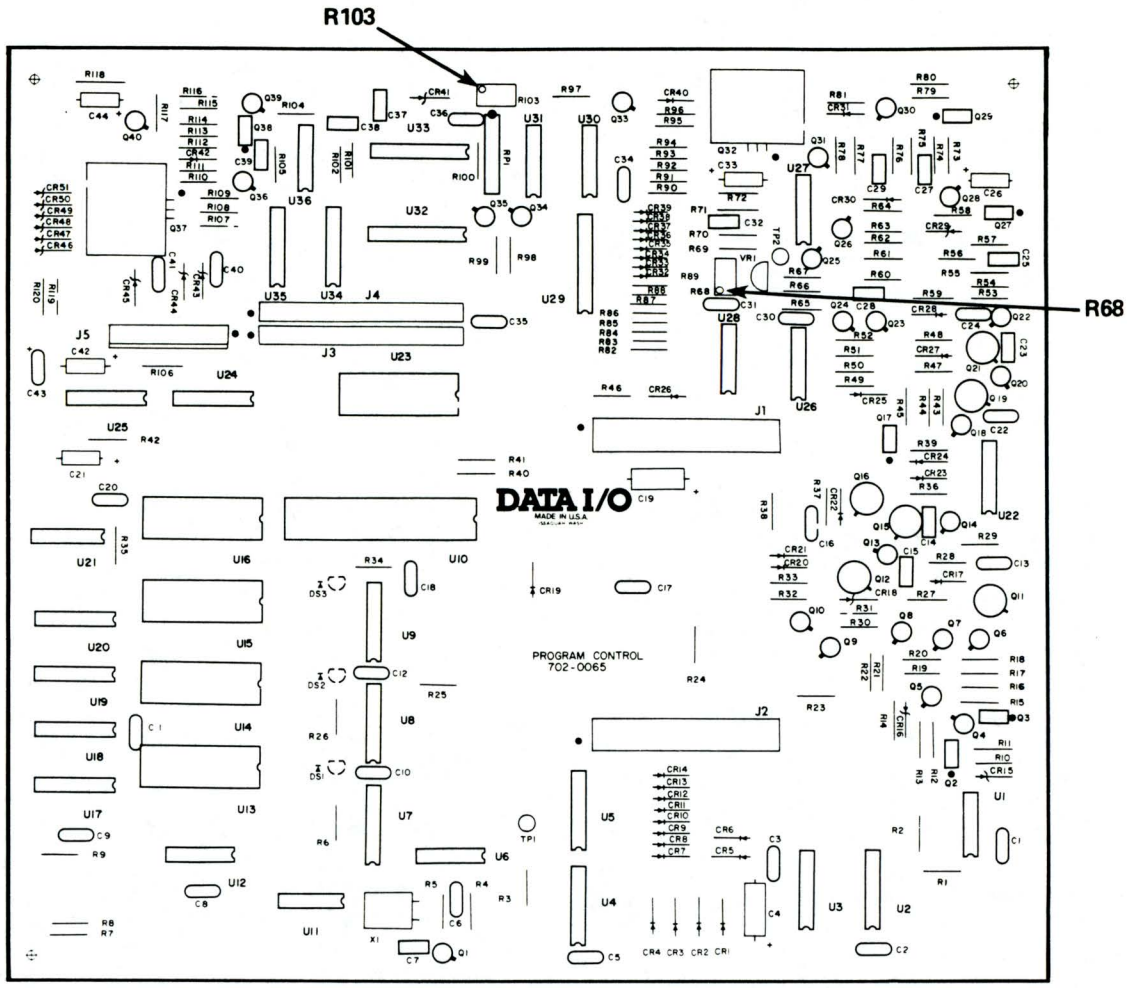


Figure 4-5. Potentiometer Locations

The minimum and maximum values for these parameters are listed in the table on the diagrams. Other voltage and timing parameters are not critical.

For waveform photographs, the trigger was set at the second graticule line from the left; by taking into account any time-base variance, you can make time comparisons between photographs. (The time base is always the same for different waveforms in the same photograph). Time-base and volts-per-division settings are printed on each photograph. The waveform names and pin numbers are called out along the edge of each photograph.

Test Procedure

a. Use the Select mode to select the PROM whose programming waveforms you wish to observe.

b. GROUP 2 ONLY: Install a master device.

c. Enter the Diagnostic mode and go to step 22.

Table 4-2. Device Groups for Waveform Observation

GROUP 1	GROUP 2
2508	2704
2516	2708
2716 (1V)	2716 (3V)
2532	48016
2732	68732-0
2732A	68732-1
	2564
2764	68764

d. Refer to the timing diagram that matches the PROM you have selected.

Measurement Chart

PROGRAMMABLE DEVICE(S) All NMOS EPROMs

DATE	REV	REVISION RECORD	DR	CK
9-22-80	A	Release	RS	

STEP	TEST NO.	TEST DESCRIPTION	TEST LOCATION		VOLTAGES			ADJUSTMENT LOCATION	COMMENTS
			SOCKETS	PINS	MIN	NOM	MAX		
1	1	VREF to +5 V	See Comments column		4.95	5.00	5.05	R68	Test location is TP2 on Controller.
									For performance check, omit this test.
	2	All Sockets Off	Both	All	-0.4	0.0	0.4	---	For steps with no adjustment location,
									if voltage is out of tolerance, see
									Introduction to Section 4.
2	3	VCC to +5 V	Both	26 and 28	4.75	5.00	5.25	---	
3	4	VCC to +5 V	Master	26 and 28	4.75	5.00	5.25	---	
	5	VCC to +12 V	Copy	26 and 28	11.4	12.0	12.6	---	
4	6	VPP to +5 V	Both	1	4.75	5.00	5.30	---	If out of range, make adjustment in
									test 9 and then recheck.
	7	VCC to +5 V	Both	26 and 28	4.75	5.00	5.25	---	
5	8	VPP to +5 V	Master	1	4.75	5.00	5.25	---	
	9	VPP to +25 V	Copy	1	24.0	25.3	26.0	R103	Adjust R103 for Copy socket only.
6	10	VPP to +5 V	Master	1	4.75	5.00	5.25	---	
	11	VPP to +26 V	Copy	1	25.0	26.3	27.0	---	
7	12	Pin 20 High	Copy	20	4.00	5.00	5.25	---	
8	13	Pin 20 to +26 V	Copy	20	25.0	26.0	27.0	---	
9	14	Pin 20 to 0 V	Both	20	-0.4	0.0	0.4	---	
	15	Pin 22 High	Copy	22	4.00	5.00	5.25	---	
10	16	Pin 22 to +12 V	Copy	22	11.4	12.0	12.6	---	
11	17	Pin 22 to +26 V	Copy	22	25.0	26.0	27.0	---	
12	18	Pin 22 to 0 V	Both	22	-0.4	0.0	0.4	---	
	19	Pin 23 to -5 V	Both	23	-5.25	-5.00	-4.75	---	

NOTES: Ground negative lead of DVM to socket pin 14.

Measurement Chart

PROGRAMMABLE DEVICE(S) All NMOS EPROMs

DATE	REV	REVISION RECORD	DR	CK
		See sheet one		

STEP	TEST NO.	TEST DESCRIPTION	TEST LOCATION		VOLTAGES			ADJUSTMENT LOCATION	COMMENTS
			SOCKETS	PINS	MIN	NOM	MAX		
13	20	Pin 23 High	Both	23	4.00	5.00	5.25	---	
14	21	Pin 23 to +5 V	Master	23	4.75	5.00	5.25	---	
	22	Pin 23 to +26 V	Copy	23	25.0	26.0	27.0	---	
15	23	Pin 23 to 0 V	Both	23	-0.4	0.0	0.4	---	
	24	Pin 21 High	Both	21	4.00	5.00	5.25	---	
16	25	Pin 21 to +12 V	Both	21	11.4	12.0	12.6	---	
17	26	Pin 21 to 0 V	Both	21	-0.4	0.0	0.4	---	
	27	Data Lines High	Both	11-13, 15-19	3.00	5.00	5.25	---	
18	28	Master Pins High	Master	3,5,7,9,11,13,15,17,	3.00	5.00	5.25	---	
				19,21,25,27					
	29	Master Pins Low	Master	2,4,6,8,10,12,14,16,	-0.4	0.0	0.4	---	
				18,20,22,24					
	30	Master Pins Other	Master	1,23,26,28	-0.4		2.0	---	
	31	Copy Pins High	Copy	All odd pins	3.00	5.00	5.25	---	
	32	Copy Pins Low	Copy	All even pins	-0.4	0.0	0.4	---	
19	33	Master Pins High	Master	1,2,4,6,8,10,12,16,18,	3.00	5.00	5.25	---	
				20,22,24,26,28					
	34	Master Pins Low	Master	3,5,7,9,11,13,14,15,17,	-0.4	0.0	0.4	---	
				19,21,23,25,27					
	35	Copy Pins High	Copy	2,4,6,8,10,12,16,18,20,	3.00	5.00	5.25	---	
				22,24,26,28					
	36	Copy Pins Low	Copy	All odd pins & pin 14	-0.4	0.0	0.4	---	
20	37	VPROG Ramp	See Comments column		---	---	---	---	Waveform photos give instructions.

NOTES: Ground negative lead of DVM or scope to socket pin 14.

Measurement Chart

PROGRAMMABLE DEVICE(S) All NMOS EPROMs

DATE	REV	REVISION RECORD	DR	CK
		See sheet one		

STEP	TEST NO.	TEST DESCRIPTION	TEST LOCATION		VOLTAGES			ADJUSTMENT LOCATION	COMMENTS
			SOCKETS	PINS	MIN	NOM	MAX		
21	38	VCC Ramp	See Comments column		---	---	---	---	Waveform photos give instructions.
22	39	Programming Waveforms	See Comments column		---	---	---	---	Waveform photos give instructions.

NOTES: Ground negative lead of DVM or scope to socket pin 14.

e. Refer to the NOTES on the timing diagram for all set-up instructions. The table of waveform variables used for each timing diagram shows the allowable time and voltage ranges and where to measure each waveform.

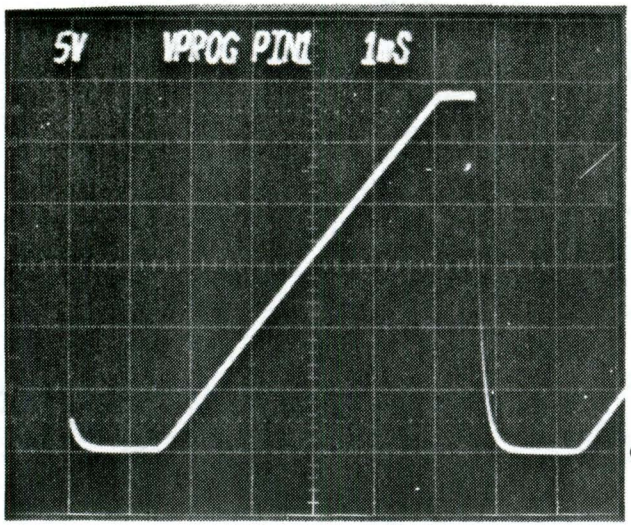
f. Observe all the waveforms indicated on the timing diagram. Compare them with the waveform photographs.

g. Repeat the procedure starting from step a if you wish to observe waveforms for other PROMs.

h. If the waveforms are not within tolerance, refer to Section 6, Troubleshooting.

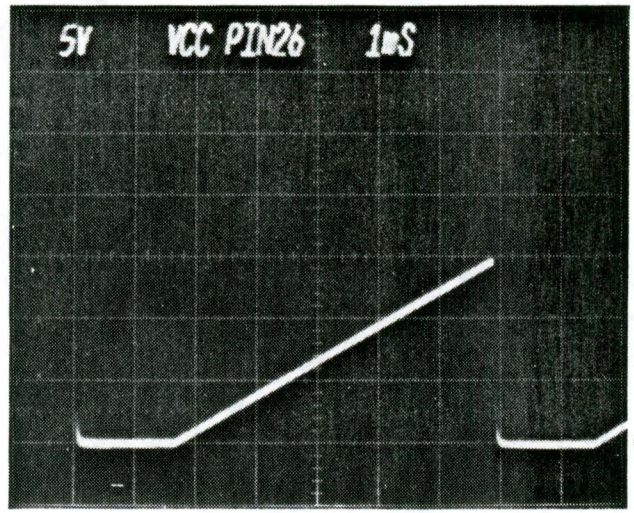
NOTE

In step 22, "22" will not appear on the display. Instead, the display will start counting down from hex 64 or hex FF, depending on the selected PROM.



VPROG Ramp Pin 1

1



VCC Ramp Pin 26, 28

2

NOTES

1. *Oscilloscope is triggered negative, internally.*
2. *Ground: pin 14 of device socket.*
3. *Time base and voltage are indicated on each photograph.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RKA	RSS	1-28-81
	B	Timing Correction	EF	RSS	9-17-81

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM FOR DIAGNOSTIC STEPS 20 & 21

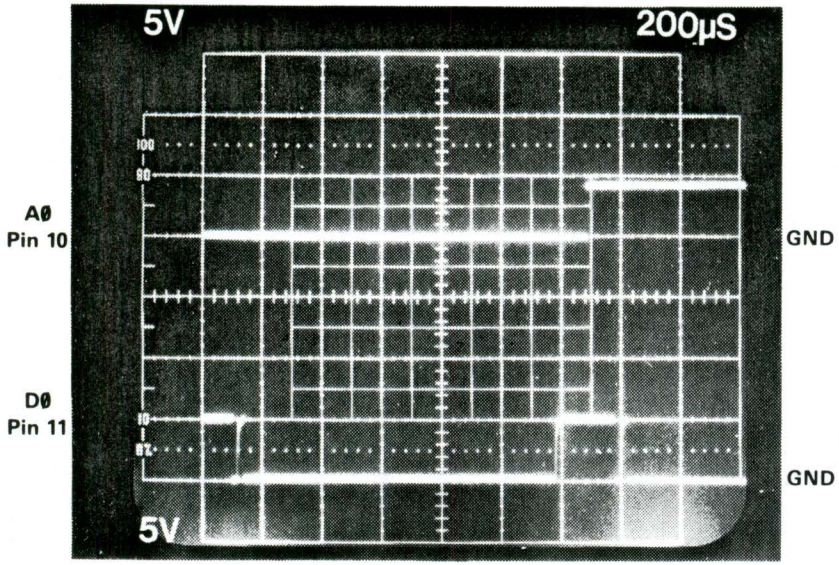
DRAWN BY: KJ

CHECKED BY:

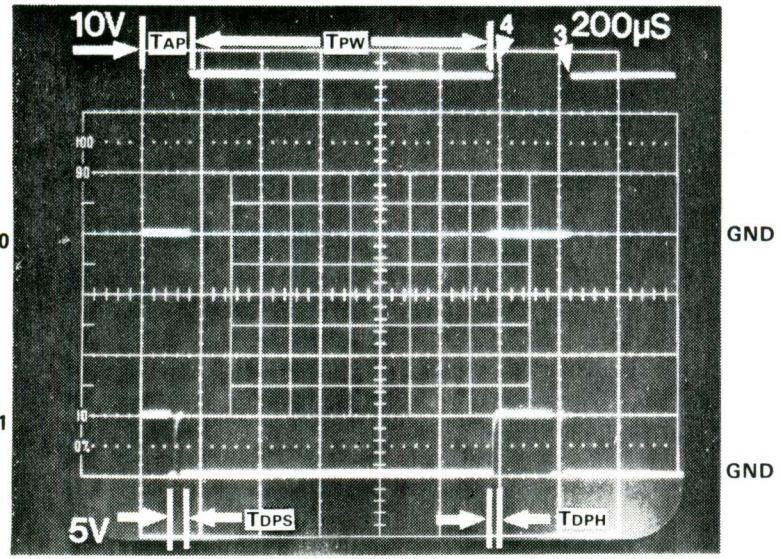
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-001

SCALE

SHEET 1/1

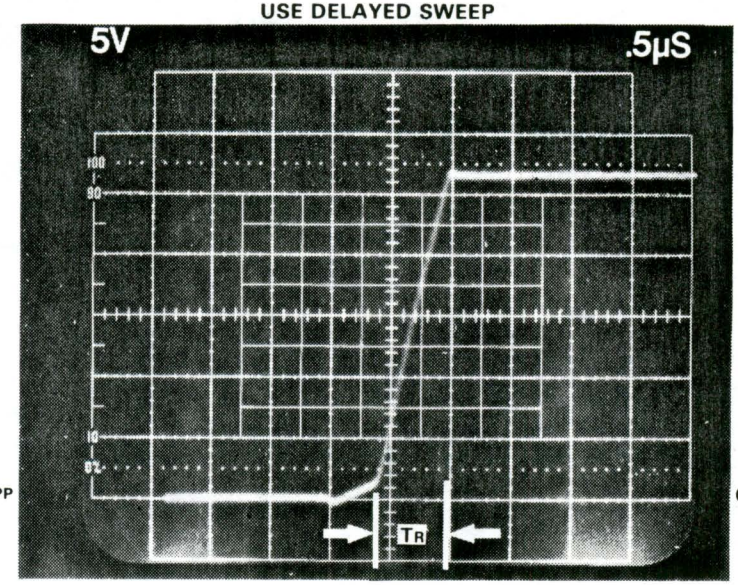


1



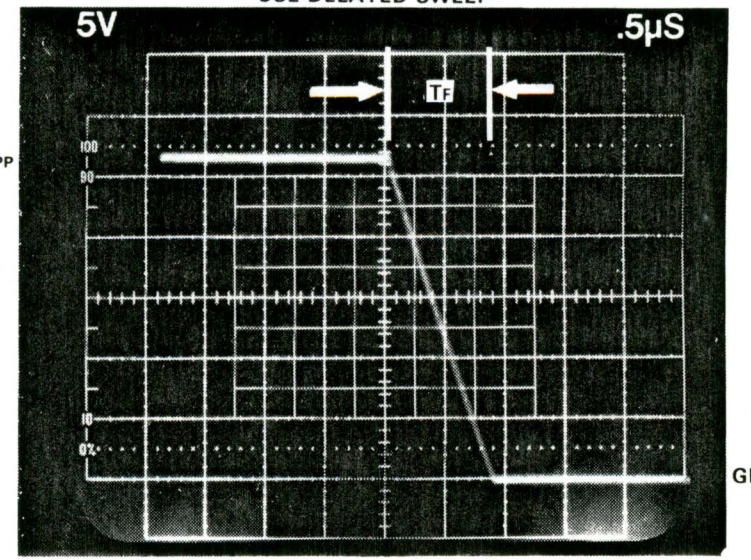
2

USE DELAYED SWEEP



3

USE DELAYED SWEEP



4

NOTES

1. *Oscilloscope trigger point: pin 10 of device socket. Trigger on negative edge. Photos 3 and 4 use delayed sweep.*
2. *Ground: pin 14 of device socket.*
3. *Time base and voltage are indicated on each photograph. The time base is the same for all waveforms in the same photograph.*
4. ► *with a number indicates a waveform section expanded to show detail. The number refers to the detailed photographs.*

WAVEFORM VARIABLES

VARIABLE	PIN	MIN	NOM	MAX	UNIT	COMMENTS
VPPH	20	25	26	27	V	
VPPL	20	−0.4	0	0.4	V	
VCC	26	4.75	5	5.25	V	
VBB	23	−5.25	−5	−4.75	V	
VDD	21	11.4	12	12.6	V	
PE	22	11.4	12	12.6	V	2704, 2708 ONLY
TPW	20	.9	1	1.1	ms	Prog. Pulse width
TAPS	20	10	—	—	us	Addr. to Prog. set-up time
TDPS	11	10	—	—	us	Data to Prog. set-up time
TDPH	11	10	—	—	us	Data to Prog. hold time
TR & TF	20	.5	1	2	us	

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RKA	RSS	1-28-81

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM, DEVICES 2704 (2126), 2708 (2127), 2716 (2328)

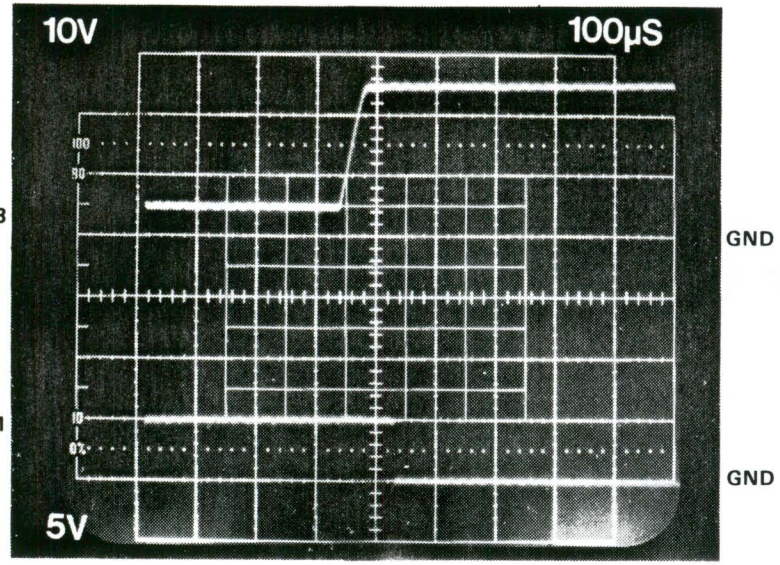
DRAWN BY: KJ

CHECKED BY: RSS

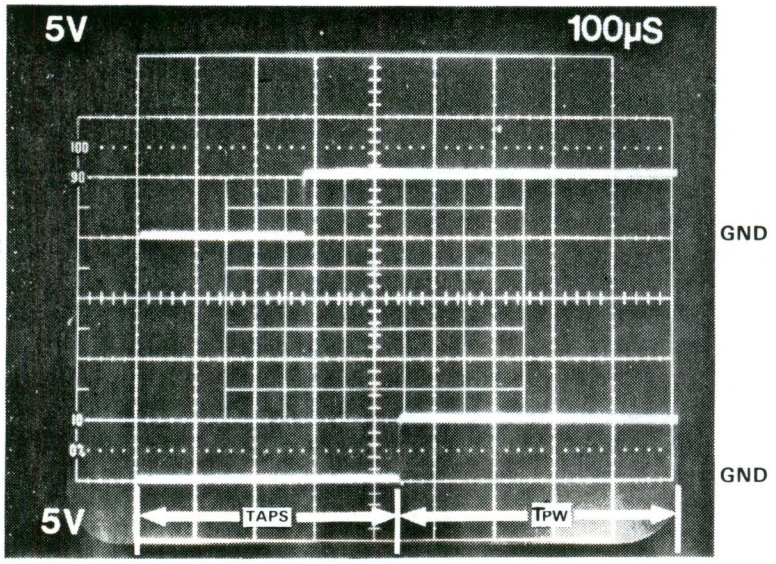
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-002

SCALE

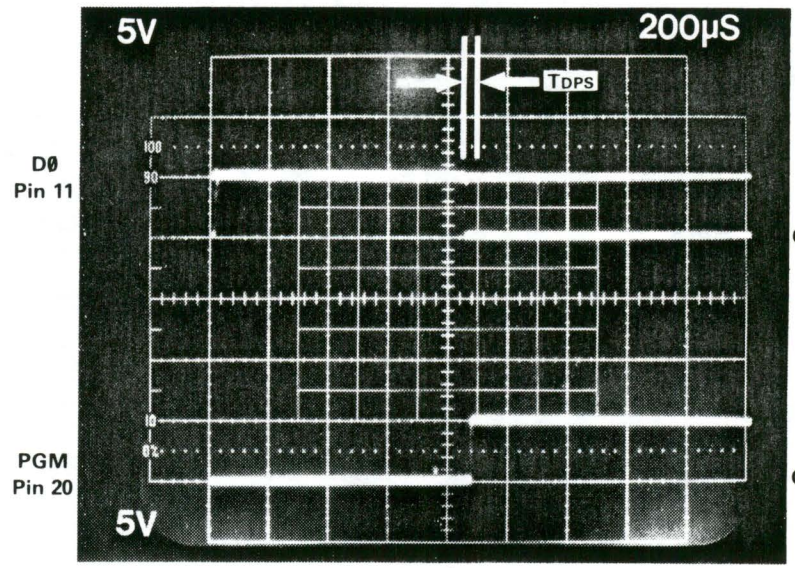
SHEET 1/1


10V
100µS
VPP
Pin 23
GND
D0
Pin 11
GND
5V

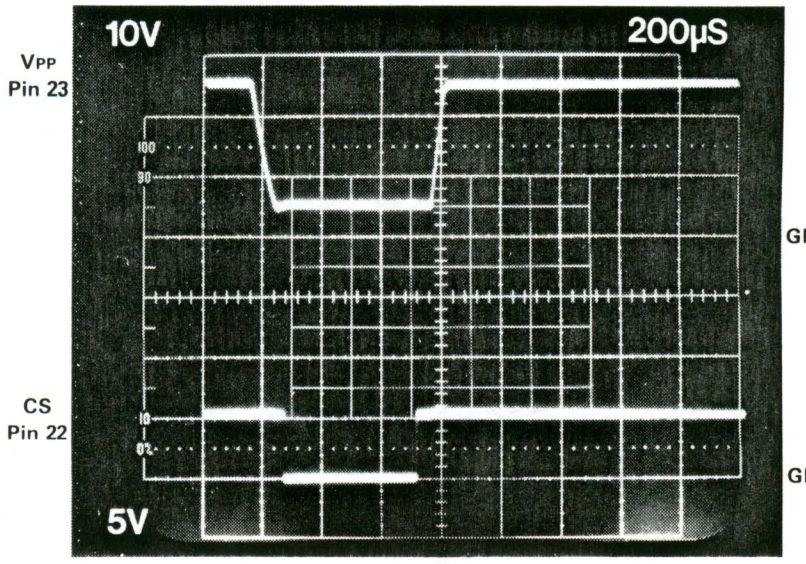
1


5V
100µS
CS
Pin 22
GND
PGM
Pin 20
GND
5V
TAPS
TPW

2


5V
200µS
TDPS
D0
Pin 11
GND
PGM
Pin 20
GND
5V

3


10V
200µS
VPP
Pin 23
GND
CS
Pin 22
GND
5V

4

NOTES

1. *Trigger points:*
   pin 10 (A0) of socket: photos 1 & 2.
   pin 20 (PGM) of socket: photos 3 & 4.

2. *Ground: pin 14 of device socket.*

3. *Time base and voltage are indicated on each photograph.*

4. ► *with a number indicates a waveform section expanded to show detail. The number refers to the detailed photograph.*

5. *All delay times are 10 us minimum.*

6. *To observe T_{PW}, turn time base down.*

WAVEFORM VARIABLES

VARIABLE	PIN	MIN	NOM	MAX	UNIT	COMMENTS
VPPH	23	24	25	26	V	
VPPL	23	4.0	5	5.25	V	
VCC	26	4.75	5	5.25	V	
TPW	20	45	50	55	ms	Prog. pulse width

4-13
10-990-0011-001

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RKA	RSS	1-26-81

DATA I/O ISSAQUAH, WA

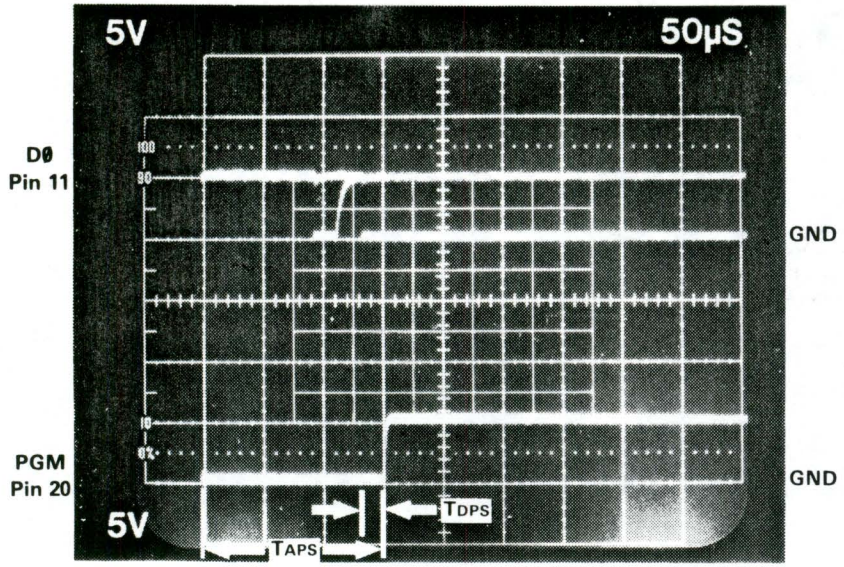
TITLE: TIMING DIAGRAM, DEVICES 2508 (1922), 2516 (1923)

DRAWN BY: KJ

CHECKED BY: RSS

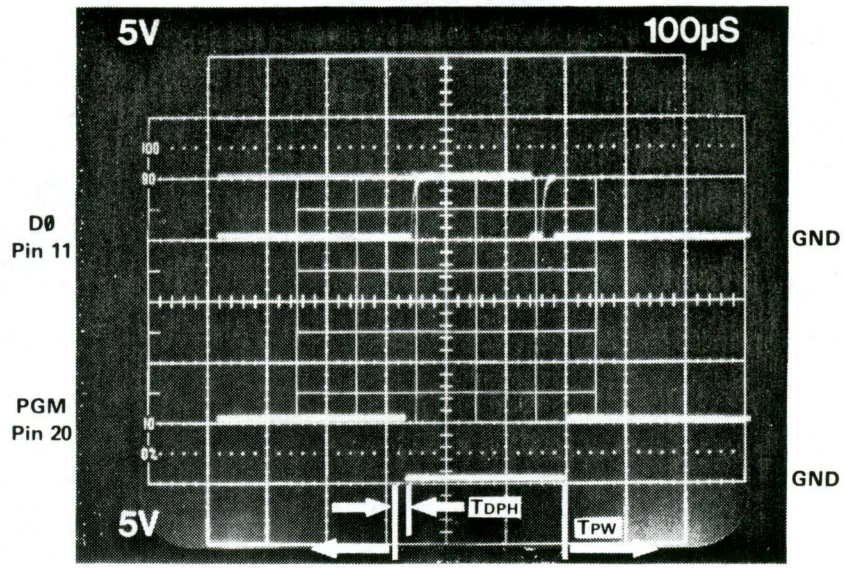
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-003

SCALE | SHEET 1/1



1

USE DELAYED SWEEP



2

NOTES

1. *In photo 1, oscilloscope trigger point is pin 10 of device socket. Trigger on negative edge. Photo 2 uses delayed sweep.*
2. *Ground: pin 14 of device socket.*
3. *Time base and voltage are indicated on each photograph.*
4. ► *with a number indicates a waveform section expanded to show detail. The number refers to the detailed photograph.*
5. *All delay times are 10 us minimum.*
6. *To observe TPW, turn time base down.*

WAVEFORM VARIABLES

VARIABLE	PIN	MIN	NOM	MAX	UNIT	COMMENTS
VPPH	23	24	25	26	V	
VCC	26	4.75	5	5.25	V	
TPW	20	9	10	11	ms	Prog pulse width

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RLA	KJ	1-28-8

DATA I/O ISSAQUAH, WA

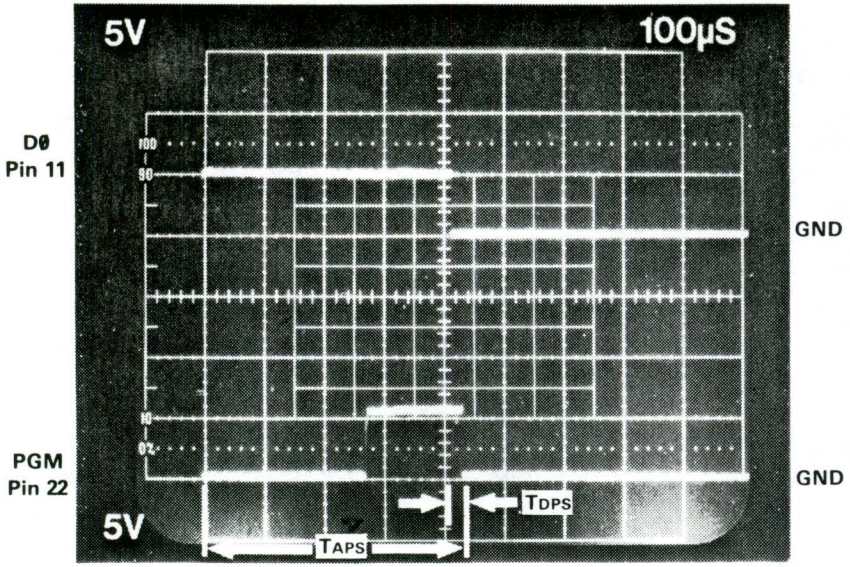
TITLE
TIMING DIAGRAM,
DEVICE 48016 (3323)

DRAWN BY: KJ

CHECKED BY:

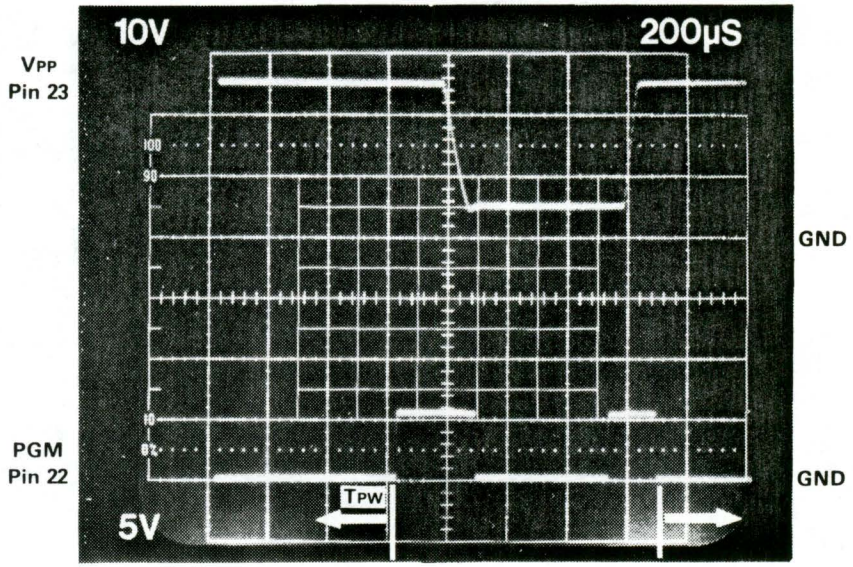
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-004

SCALE | SHEET 1/1



1

USE DELAYED SWEEP



2

NOTES

1. *In photo 1 oscilloscope trigger point is pin 10 of device socket. Trigger on negative edge. Photo 2 uses delayed sweep.*
2. *Ground: pin 14 of device socket.*
3. *Time base and voltage are indicated on each photograph.*
4. ► *with a number indicates a waveform section expanded to show detail. The number refers to the detailed photograph.*
5. *All delay times are 10 us minimum.*
6. *To observe TPW, turn time base down.*

WAVEFORM VARIABLES

VARIABLE	PIN	MIN	NOM	MAX	UNIT	COMMENTS
VPPH	23	24	25	26	V	
VPPL	23	4.0	5.0	5.25	V	
VCC	26	4.75	5.0	5.25	V	
TPW	22	45	50	55	ms	Prog. pulse width

4-17
10-990-0011-001

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RRA	CJB	1-28-84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM,
DEVICE 2532 (1925)

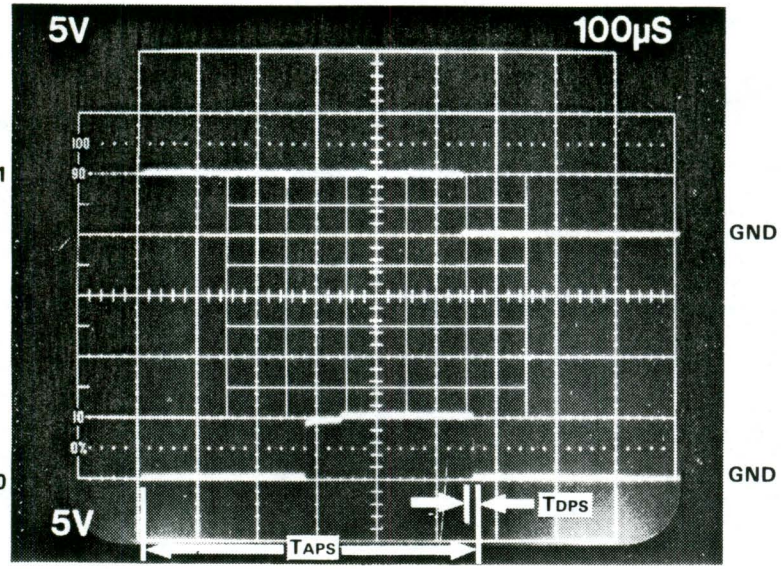
DRAWN BY: KJ

CHECKED BY: Jles

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-005

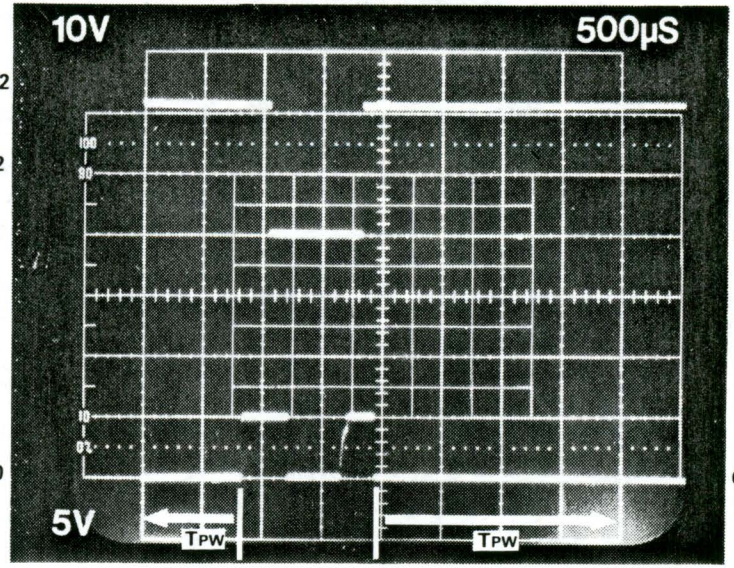
SCALE

SHEET 1/1



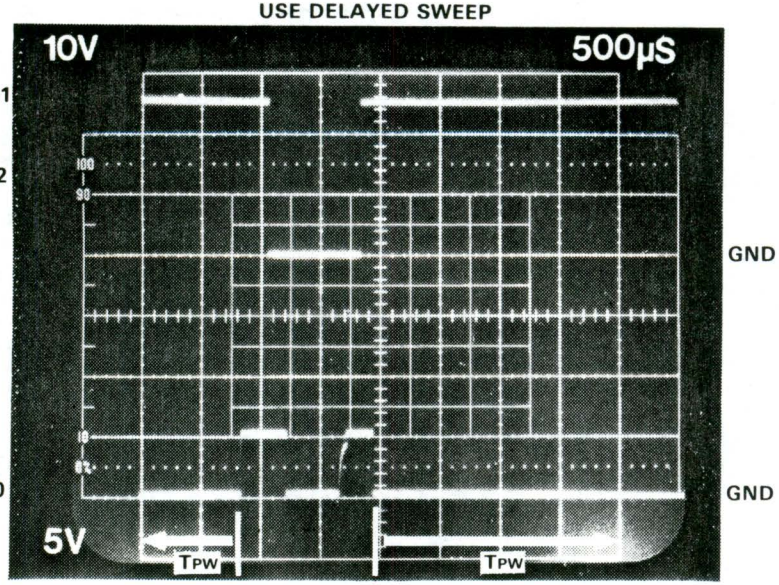
1

USE DELAYED SWEEP



3

USE DELAYED SWEEP



2

NOTES

1. *In photo 1, oscilloscope trigger point is pin 10 of device socket. Trigger on negative edge. Photos 2 and 3 use delayed sweep.*
2. *Ground: pin 14 of device socket.*
3. *Time base and voltage are indicated on each photograph.*
4. ► *with a number indicates a waveform section expanded to show detail. The number refers to the detailed photograph.*
5. *All delay times are 10 us minimum.*
6. *To observe T_{PW}, turn time base down.*

WAVEFORM VARIABLES

VARIABLE	PIN	MIN	NOM	MAX	UNIT	COMMENTS
$VPPH_1$	22	24	25	26	V	2732 ONLY Photo 2
$VPPH_2$	22	20.5	21	21.5	V	2732A ONLY Photo 3
VPPL	22	−0.4	0	0.45	V	
VCC	26	4.75	5	5.25	V	
TPW	20	45	50	56	ms	Prog. pulse width

4-19
10-990-0011-001

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RRA	RJ	1-28-81

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM, DEVICE 2732 (1924) 2732A (2724)

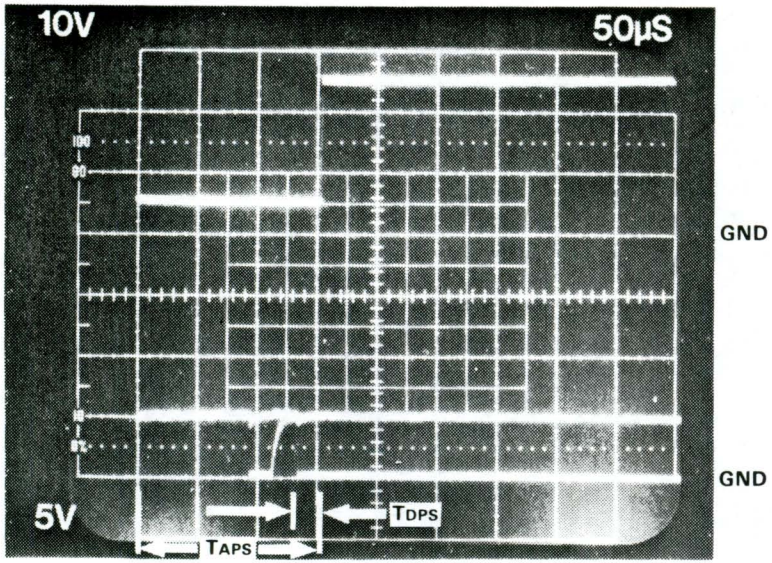
DRAWN BY: KJ

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-006

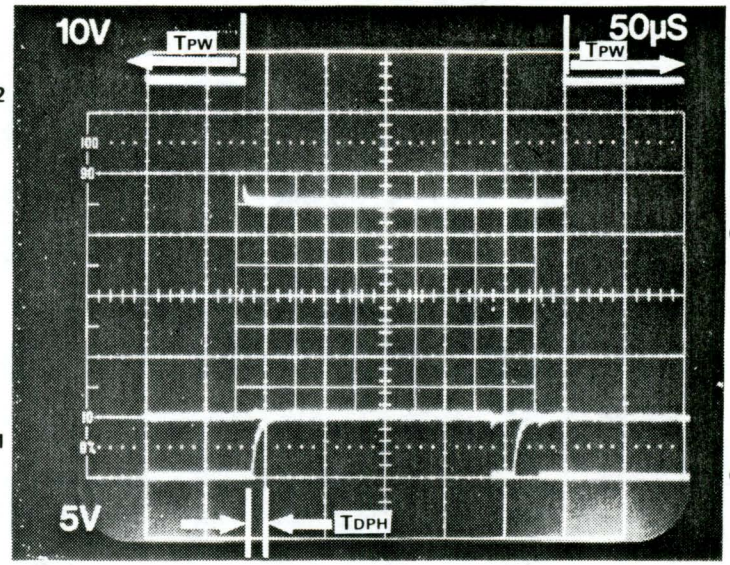
SCALE

SHEET 1/1



1

USE DELAYED SWEEP



2

NOTES

1. *In photo 1, oscilloscope trigger point is pin 10 of device socket. Trigger on negative edge. Photo 2 uses delayed sweep.*
2. *Ground: pin 14 of device socket.*
3. *Time base and voltage are indicated on each photograph.*
4. ► *with a number indicates a waveform section expanded to show detail. The number refers to the detailed photograph.*
5. *All delay times are 10 us minimum.*
6. *To observe TPW, turn time base down.*

WAVEFORM VARIABLES

VARIABLE	PIN	MIN	NOM	MAX	UNIT	COMMENTS
VPPH	22	24	25	26	V	
VPPL	22	4.0	5	5.25	V	
VCC	26	4.75	5	5.25	V	
TPW	22	1.8	2	2.2	ms	Prog. pulse width

4-21
10-990-0011-001

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RLA	RSY	1-28-81

DATA I/O ISSAQUAH, WA

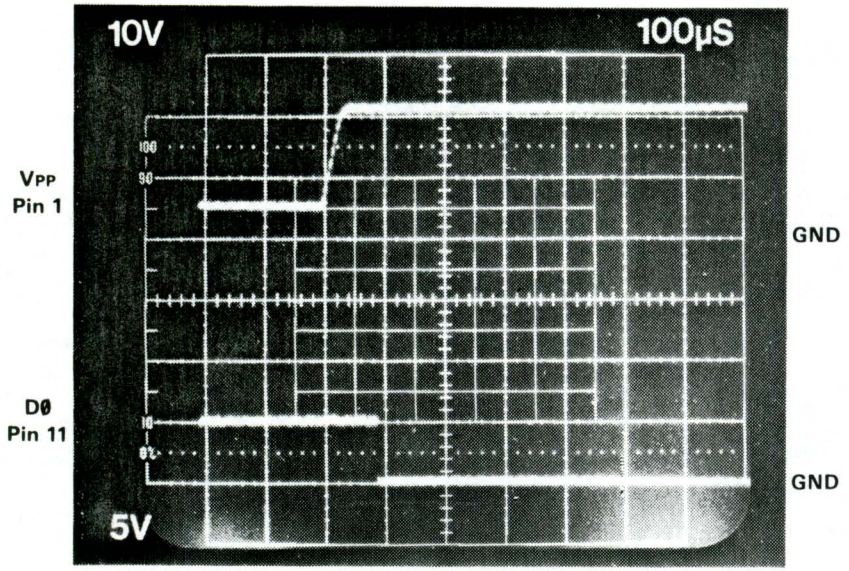
TITLE
TIMING DIAGRAM,
DEVICE 68732-0 (2544),
68732-1 (2545), 68764 (2529)

DRAWN BY: KJ

CHECKED BY:

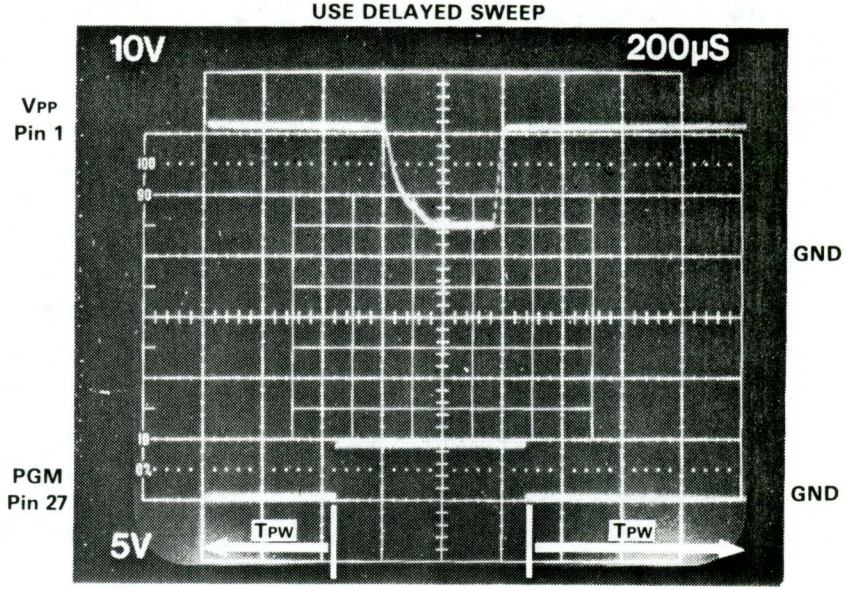
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-007

SCALE | SHEET 1/1



1

USE DELAYED SWEEP



2

NOTES

1. *In photo 1, oscilloscope trigger point is pin 10 of device socket. Trigger on negative edge. Photo 2 uses delayed sweep.*
2. *Ground: pin 14 of device socket.*
3. *Time base and voltage are indicated on each photograph.*
4. ► *with a number indicates a waveform section expanded to show detail. The number refers to the detailed photograph.*
5. *All delay times are 10 us minimum.*
6. *To observe TPW, turn time base down.*

WAVEFORM VARIABLES

VARIABLE	PIN	MIN	NOM	MAX	UNIT	COMMENTS
VPPH	1	20.5	21	21.5	V	
VPPL	1	4.0	5	5.25	V	
VCC	28	4.75	5	5.25	V	
TPW	27	45	50	55	ms	Prog. pulse width

4-23
10-990-0011-001

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RRA	RSL	1-28-81

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM, DEVICE 2764 (3533)

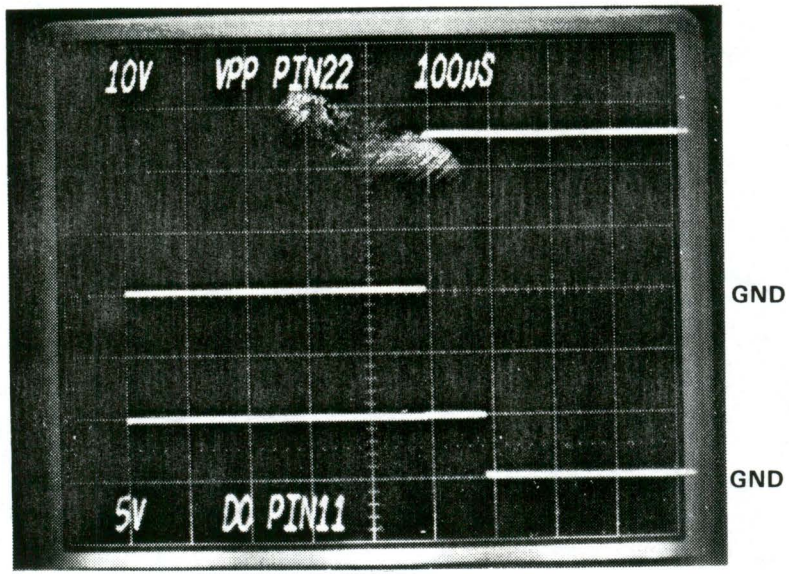
DRAWN BY: KJ

CHECKED BY:

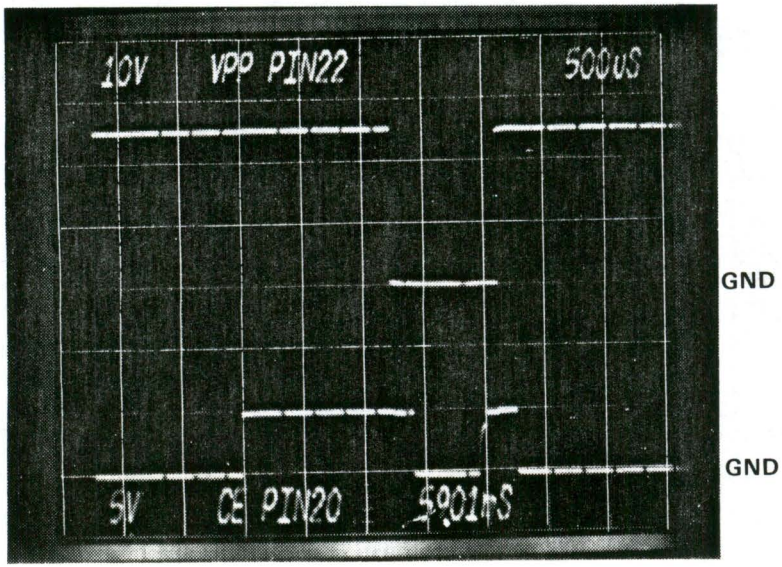
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-008

SCALE

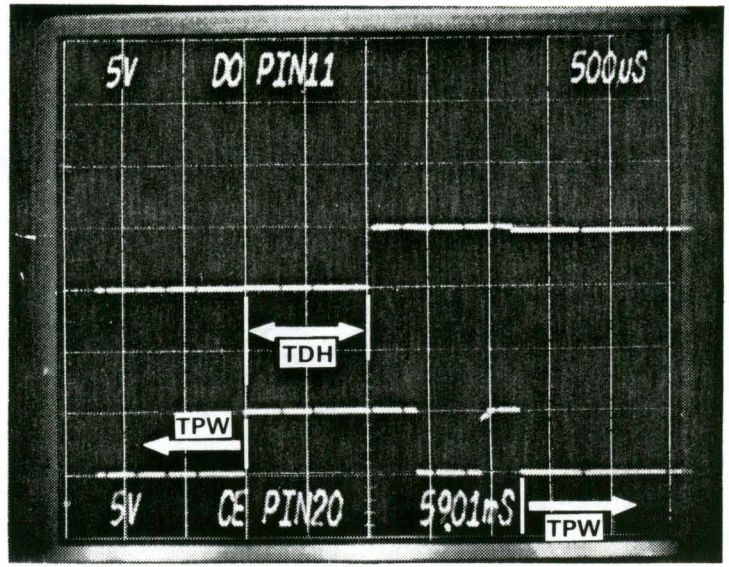
SHEET 1/1


10V VPP PIN22 100uS
GND
GND
5V DO PIN11

1


10V VPP PIN22 500uS
GND
GND
5V CE PIN20 5.01mS

2


5V DO PIN11 500uS
GND
TDH
TPW
GND
5V CE PIN20 5.01mS
TPW

3

NOTES

1. *In photo 1, oscilloscope trigger point is pin 10 of device socket. Trigger on the negative edge. Photo 2 and 3 use delayed sweep.*
2. *Ground: pin 14 of device socket.*
3. *Time base and voltage are indicated on each photograph.*
4. *► with a number indicates a waveform section expanded to show detail. The number refers to the detailed photograph.*
5. *All delay times are 10 us minimum, except TDH and TAH.*
6. *To observe T_{PW}, turn time base down.*

WAVEFORM VARIABLES

VARIABLE	PIN	MIN	NOM	MAX	UNIT	COMMENTS
VPPH	22	24	25	26	V	
VPPL	22	−0.4	0	0.4	V	
VCC	28	4.75	5	5.25	V	
TPW	20	9	10	11	ms	Prog. pulse width
TDH	11	1			ms	Data hold time
TAH		1			ms	Address hold time (Not shown)

4-25
10-990-0011-001

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	B	ECN #4261	CF	RLS	3/11/81

DATA I/O ISSAQUAH, WA

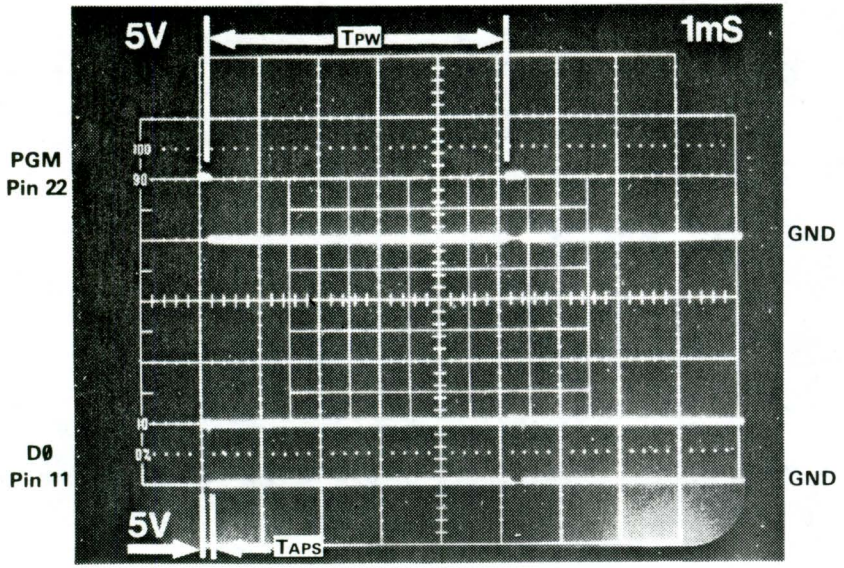
TITLE
TIMING DIAGRAM
DEVICE 2764 (4539)

DRAWN BY: KT

CHECKED BY: DC

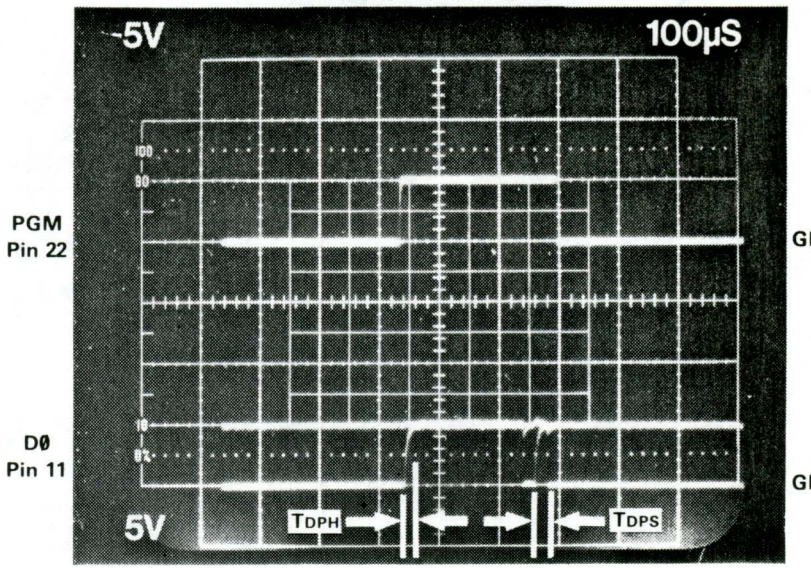
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-009

SCALE | SHEET 1/1



1

USE DELAYED SWEEP



2

NOTES

1. *In photo 1, oscilloscope trigger point is pin 10 of device socket. Trigger on negative edge. Photo 2 uses delayed sweep.*
2. *Ground: pin 14 of device socket.*
3. *Time base and voltage are indicated on each photograph.*
4. *► with a number indicates a waveform section expanded to show detail. The number refers to the detailed photograph.*
5. *All delay times are 10 us minimum.*

WAVEFORM VARIABLES

VARIABLE	PIN	MIN	NOM	MAX	UNIT	COMMENTS
VPPH	1	24	25	26	V	
VPPL	1	4.0	5.0	5.25	V	
VCC	28	4.75	5.0	5.25	V	
TPW	1	4.5	5	5.5	ms	Prog. pulse width

4-27
10-990-0011-001

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
	A	RELEASE	RAH	RSS	1-28-81

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM, DEVICE 2564 (3130)

DRAWN BY: KJ

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-990-0010-010

SCALE

SHEET 1/1

SECTION 5
MAINTENANCE

5.1 INTRODUCTION

The primary maintenance requirement is for periodic cleaning of the Model 20B's cooling vents to make sure that airflow through the vents is not impeded. Except for this precaution, the outside of the unit should be checked routinely for dust or dirt, and the inside should be checked for cables or other components that may have become unseated.

A good time to schedule cleaning and inspection is before every calibration.

5.2 CLEANING

Clean the outside of the unit with a mild detergent on a damp cloth or brush. Never use caustic or abrasive agents; these will damage the Model 20B.

5.3 INSPECTION

Check cable connections, card seating, mounting of socketed components, etc., for shorts, opens or unstable continuity. Use particular care if you find heat-damaged components. It is important to find and correct the cause of overheating in order to prevent recurrence of the damage. If you find parts damaged through overheating, consult Section 6, Troubleshooting.

SECTION 6
TROUBLESHOOTING

6.1 INTRODUCTION

The following information is an aid to interpreting malfunctions and locating hardware failures in the Model 20B. The troubleshooting procedures below will help to isolate errors to specific areas.

Refer to Figure 6-1. As the flowchart shows, you should always calibrate the programmer before troubleshooting, unless a machine error has made calibration impossible. By calibrating the programmer first, you might solve the problem or at least isolate the problem to one functional area or even down to a few components.

After successful troubleshooting, recalibrate the programmer.

6.2 CALIBRATION ERRORS

If you discover errors that cannot be corrected by calibration, do the following:

- If a **power supply** is out of range, troubleshoot the power supplies according to Table 6-1.
- If a **DC voltage** is out of range, troubleshoot the problem according to Table 6-2.
- If **waveforms** do not match those on the timing diagrams, contact your local Data I/O Service Center.

6.3 SYSTEM DOES NOT OPERATE OR OPERATES ERRATICALLY

CAUTION

Use safe electrical procedures whenever you are working within this unit. Improper handling of the circuitry may injure the operator or damage this unit. Only qualified electronics personnel should attempt to calibrate or troubleshoot this unit.

If the programmer does not power up, or if it operates erratically, complete the following steps. After completing each step, determine whether the problem still exists.

a. Check that the AC power cord is firmly plugged in and the ON/OFF switch is on and, check the AC fuse at the back of the unit.

b. Locate J2 on the Power Supply Board and J4 on the Program Control Board. Check that the power supply cable is inserted fully at both ends and in the right direction. Pin 1 of the cable is identified by the red dot. Pin 1 of the connectors is identified by the white dot next to each connector.

c. Check that all other cables are inserted fully and in the right direction.

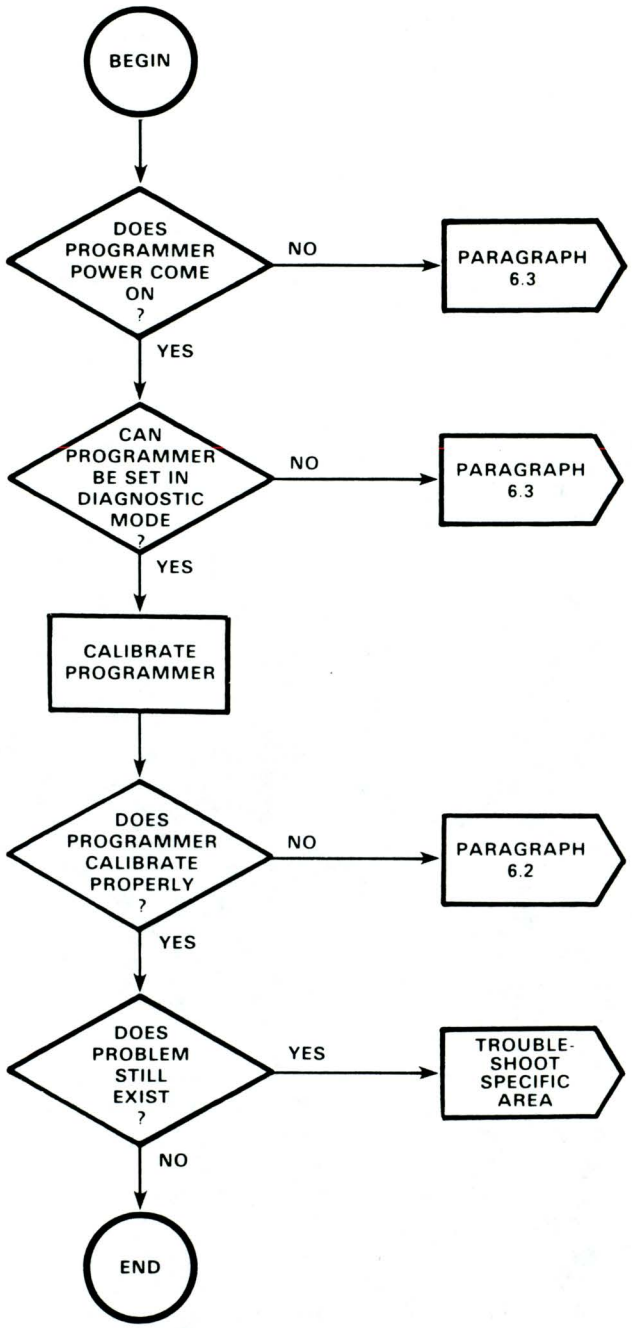


Figure 6-1. Troubleshooting Flowchart

d. TURN THE AC POWER SWITCH OFF and remove the AC cord. Locate the 15-pin commoning block, which is on the inside of the back panel just above the fuse holder. Press firmly on each wire which connects to the block; a wire may have worked loose. Attach the AC cord. Then turn the AC power switch on again.

e. Check fuses F1-F5 on the Power Supply Board. A blown fuse indicates the need for further troubleshooting. Replace the blown fuse and determine the cause of the blown fuse before programming PROMs again.

Table 6-1. Power Supply Troubleshooting

SUPPLY	VOLTAGE RANGE Min.	Nom.	Max.	TEST LOCATION ON J2	NOTES	SUSPECT COMPONENTS
+38 V	34.0	38.0	48.0	Pin 1		C5, CR5-CR8, F3, F5
Gnd. Sense	-0.4	0.0	0.4	Pin 2		VR2
+5 V	4.75	5.00	5.25	Pin 3	For this test only, short pin 2 to pin 6 on free end of cable.	C1, C7, C10, CR2, CR4, F1, F2, VR2
+12 V	11.4	12.0	12.6	Pin 4		C2, C6, C8, CR6, CR8, F3-F5, VR1
-14 V	-15.5	-14.0	-9.0	Pin 5		C3, C4, CR1, CR3, F1, F2, VR3
Gnd.	-0.4	0.0	0.4	Pin 6		
-5 V	-5.25	-5.00	-4.75	Pin 7		C3, C4, C9, CR1, CR3, F1, F2, VR3
+19 V	16.0	19.0	24.0	Pin 8		C2, C6, CR6, CR8, F3-F5, VR1

SET-UP INSTRUCTIONS

1. Remove cable from J5 on Program Control Board.
2. Connect negative lead of DVM to system ground.
3. All test locations are at J2 on Power Supply Card.
4. Check components in last column if test fails.
5. After all tests are done, reattach cable to Program Control Board.
6. If voltages are within range, troubleshoot Program Control Board.

f. Locate the program PROMs (U13-U16) on the Program Control Board. (There may be less than 4 PROMs.) Check that each PROM is fully inserted in its socket and that none of the PROMs are damaged or installed backwards.

g. Inspect all other components on the Program Control Board. Make sure that all socketed components are properly seated; make sure that all soldered components are intact. Also, check that the cable from the Keyboard/Display Board is not shorting to the Program Control Board.

h. If steps a—g do not reveal the problem, contact your local Data I/O Service Center.

6.4 SERIAL I/O FAILURE

If serial I/O data transfers do not work or are erratic, complete the following steps. After completing each step, determine whether the problem still exists.

a. Locate the baud rate switch, U4 on the Serial I/O Board. Segments 1 through 7 of U4 set the baud rate. Check that only one of the switches is on. Figure 2-2 shows the baud rate for each setting. Check that the baud rate on the programmer and the peripheral are set the same.

b. Check that both instruments are set for the same parity and number of stop bits.

c. Use an oscilloscope to measure the clock input to the Serial I/O Board at U5 pin 2. The pulse period should be 271 ns. Suspect component: 22-pin flat cable to Serial I/O Board.

d. Check the signal at U5 pin 12. The period should be 1.628 *us*. Suspect components: U5, U6

e. Refer to Table 6-3. Measure the clock signal at U9 according to the table. Suspect components: U3, U6, U7

Table 6-2. DC Voltage Troubleshooting

MEASUREMENT CHART TEST NUMBER	SUSPECT COMPONENTS ON PROGRAM CONTROL BOARD
1	U3, U28, VR1
2	---
3	U27, U32, U35, U36, Q32, Q35-37
4	U27, U32, U35, Q36, Q37
5	U27, U32, U35, U36, Q36, Q37
6	U32, U34, U36, Q38-40
7	U27, U32, U35, U36, Q32, Q35-37
8	U27, Q32-35
9	U32, U34, U36, Q38-40
10	U27, Q32-35
11	U32, U34, U36, Q38-40
12	U3, U22, Q5, Q12, Q13, CR17
13	U3, U22, Q5, Q12, Q13, CR17
14	U3, U22, Q5, Q12, Q13, CR17
15	U2, U22, U28, Q16
16	U2, U22, U28, Q16
17	U2, U22, U28, Q16
18	U2, U22, U28, Q16
19	U2, U4, U26, U27, Q21-24
20	U3, U4, U26, Q21, Q23, Q24
21	U1, Q2-4, CR15
22	U3, Q6, Q18-20, R4
23	U1, U3, Q2-4, Q6, Q18-20, CR15, R4
24	U4, U26, Q17
25	U2, U26, U27, Q29, Q31, CR25
26	U2, U26, U27, Q29, Q31, CR25
27	U3, U27-32, CR32-39, Q32, Q34, Q35
28	U4, U5, U29-32
29	U4, U5, U29-32
30	U4, U5, U29-32
31	U4, U5, U29-32
32	U4, U5, U29-32
33	U4, U5, U29-32
34	U4, U5, U29-32
35	U4, U5, U29-32
36	U4, U5, U29-32
37	U32, U34, U36, Q38-40
38	U32, U35, U36, Q36, Q37

Table 6-3. Required Clock Periods on the ACIA

SWITCH SETTING ON U4	MEASUREMENT LOCATION	CLOCK PERIOD
Segment 1 on	U9 pin 3	1.628 *us*
Segment 2 on	U9 pin 3	3.256 *us*
Segment 3 on	U9 pin 3	6.51 *us*
Segment 4 on	U9 pin 3	13.02 *us*
Segment 5 on	U9 pin 3	26.04 *us*
Segment 6 on	U9 pin 3	52.08 *us*
Segment 7 on	U9 pin 3	143.2 *us*

f. If steps a—e do not reveal the problem, contact your local Data I/O Service Center.

6.5 ERRATIC DISPLAY

If one digit on the display or one segment of a digit does not light up, check digit drivers Q1 through Q4 or segment drivers U1 and U2 on the Keyboard/Display Board. Replace if necessary.

If this does not solve the problem, contact your local Data I/O Service Center.

SECTION 7
CIRCUIT DESCRIPTION

7.1 INTRODUCTION

This section describes the circuitry of the Model 20B's main components. It also defines the system address map, control timing and architecture. Each circuit card assembly is described separately in terms of its functions.

7.2 GENERAL ARCHITECTURE

The Model 20B programmer is a microprocessor-based system designed around the type 6802 microprocessor. The 6802 is located on the Program Control Board and controls circuitry on the board which produces internal digital control and analog waveforms. Interfacing with the Program Control Board are the Power Supply Board, Socket Board, Keyboard/Display Board and Serial I/O Board. See Figure 7-1.

7.3 WRITE AND READ TIMING

Timing for a write operation is shown in Figure 7-2. Timing for a read operation is shown in Figure 7-3.

7.4 MEMORY MAP

The memory map in Table 7-1 shows the location in hexadecimal of each decoded function of the Model 20B.

7.5 MAIN COMPONENTS

The circuitry of each of the Model 20B's main components is described in paragraphs 7.5.1 through 7.5.5. The schematic for each board is in Section 9.

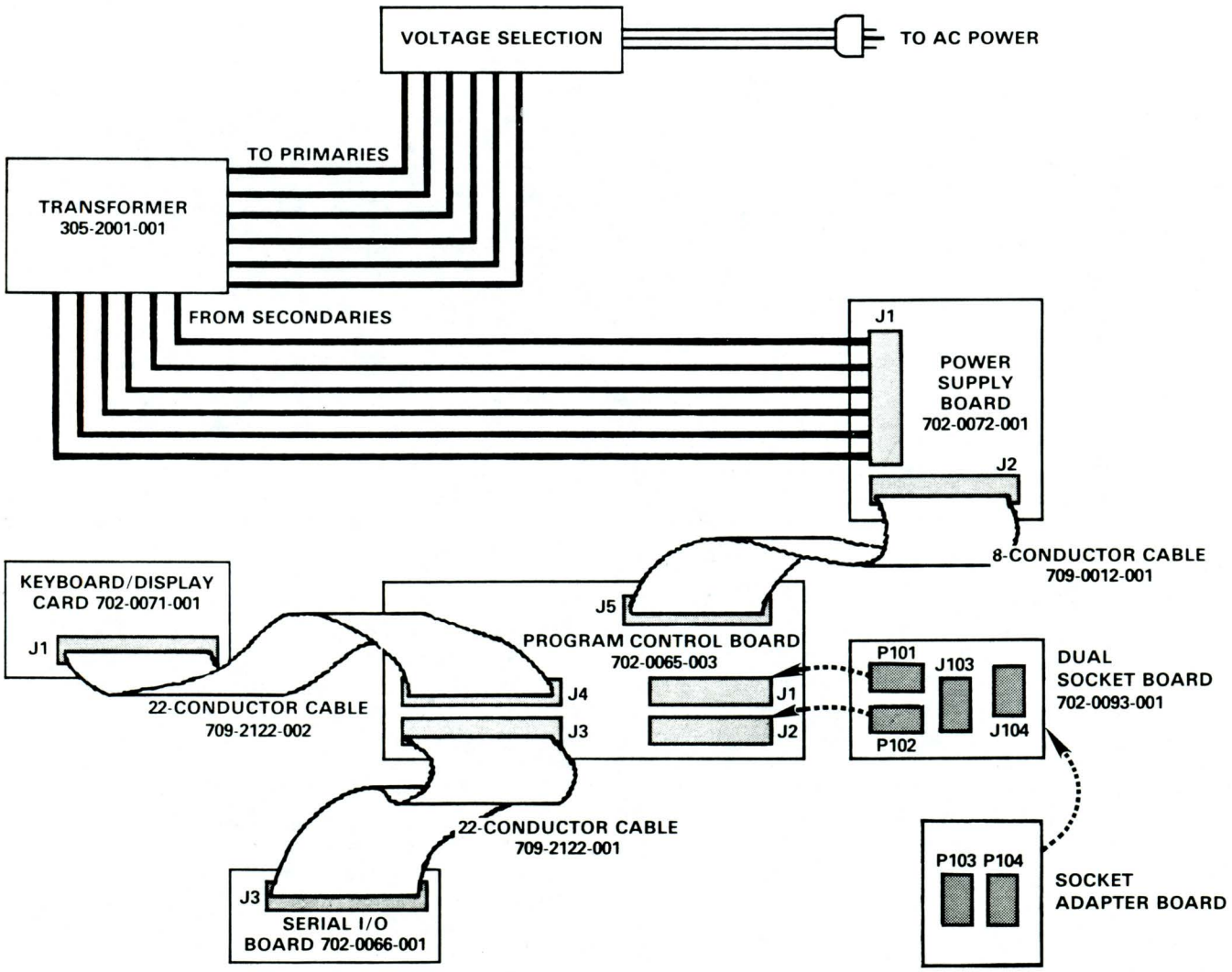


Figure 7-1. Card Interconnection Diagram

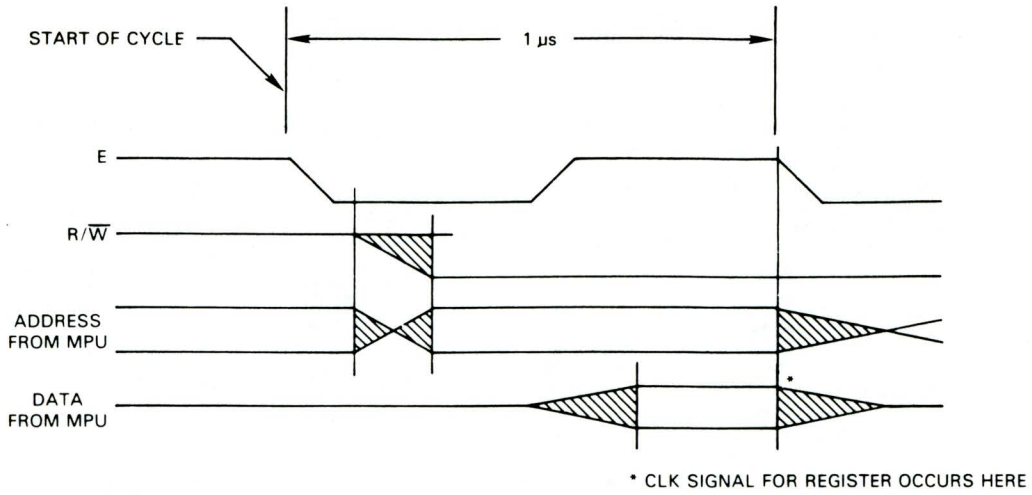


Figure 7-2. Write Timing

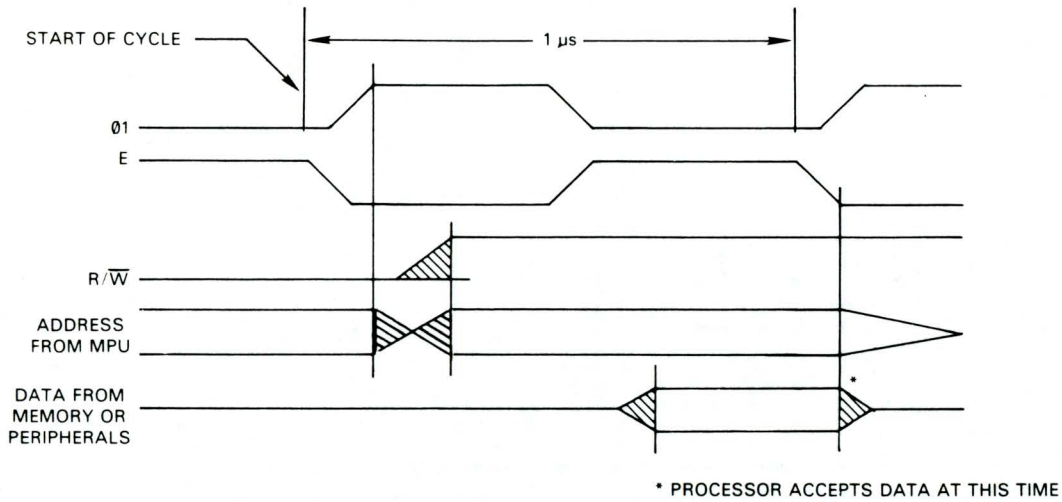


Figure 7-3. Read Timing

Table 7-1. Memory Map

ADDRESS RANGE	FUNCTION
0000-007F	Scratch RAM, 6802
0080-00FF	Scratch RAM, 6810
0400-0401	Keyboard/display interface, 8279
0800-0801	Serial port, 6850
1800-1BFF	Data RAM, lower half, 2114
1C00-1FFF	Data RAM, upper half, 2114
8000-8007	Address register, low order, 74LS259
8008-800F	Address register, high order, 74LS259
8010-8017	Control register 1, 74LS259
8018-801F	Control register 2, 74LS259
8020	Program voltage DAC, AD7524
8038	Data driver, 74LS374
8800	Status read gates, 74LS126
9000	Vcc DAC, AD7524
9800	Data read gates, 74LS244
A000-A7FF	Program memory, 2716
A800-AFFF	Program memory, 2716
B000-B7FF	Program memory, 2716
B800-BFFF	Program memory, 2716

7.5.1 POWER SUPPLY

Refer to the schematics in Section 9.

The Power Supply Board (702-0072-001) contains the rectifier, filter, and regulator circuits that produce the +5 V, −5 V and +12 V supplies. This board also produces unregulated +38 V, +19 V, and −14 V supplies for use by the Program Control Board.

Input to the Power Supply Board comes from the transformer secondary windings. The primaries connect to the AC-power wiring block. All power supplies are protected by 2 A, fast-blow fuses, F1−F5.

7.5.2 PROGRAM CONTROL BOARD

Refer to Figure 7-4.

The Program Control Board (702-0065-003) is controlled by a 6802 microprocessor (U10), which contains 128 bytes of scratch memory. Additional scratch memory is provided by a 6810 RAM, U23.

At POWER-ON a one-shot (U25) resets the 6802 and a crystal-controlled clock signal is applied to the 6802. The processor's address lines are decoded by 74LS138 decoders

(U8, U9 and U24) to produce the enable signals necessary for access to the other memory and I/O devices on the bus.

INSTRUCTIONS TO THE 6802 are fetched from program memory, which consists of up to four 2Kx8 2716 EPROMs (U13-U16). Data is stored into 2K bytes of 2114 data RAM (U17-U20). Hold buffer U7 extends the valid address time for the three low-order address lines, allowing access to the 74LS259 addressable latches; hold buffer U32 extends the valid data time for the eight data lines, allowing access to the AD7524 D-to-A converters (U34 and U35).

DC POWER from the Power Supply Board is sent to the Program Control Board through power distribution circuits which contain zener diode overvoltage protection and bypass capacitors. Two additional supplies for op amp power, +30 V and -9 V, are located on the Program Control Board.

PROM ADDRESSES are written into two 74LS259 addressable latches (U4 and U5) and then sent to the Socket Board. PROM data is written into the data driver, a 74LS374 octal flip-flop, and sent to the data lines on the socket board. When data is read from the Socket Board, the data driver is disabled and the data from the Socket Board is sent through the data pullup and pulldown resistors (R82-R89) and the data comparators (U30 and U31) to the data read gates (U33). From the read gates the data can be accessed by the processor.

For SIGNAL CONTROL on the Socket Board, the processor writes to two 74LS259 control registers (U2 and U3). The outputs of these control registers, the control lines, turn on the socket supplies and switches.

The SOCKET SUPPLIES consist of: the V_{PROG} supply and the V_{CC} supply, both controlled by D-to-A converters; the V_{DD} supply for +12 volts; the V_{BB} supply for -5 volts; and the master V_{CC} supply for +5 volts. These voltages are applied to the switching networks, which direct the supply voltages to the proper socket pins. The switching networks, designated the pin 20, pin 21, pin 22 and pin 23 drivers, are turned on by the current sources (Q4-Q7). The socket supplies are all interconnected to the overcurrent shutdown circuit.

An overcurrent at the sockets will clear the address registers (U4 and U5) and the control registers (U2 and U3), causing all supplies and switches to turn off. The processor reads the status gates to determine if either an overcurrent shutdown has occurred or all the supplies and switching networks are turned on.

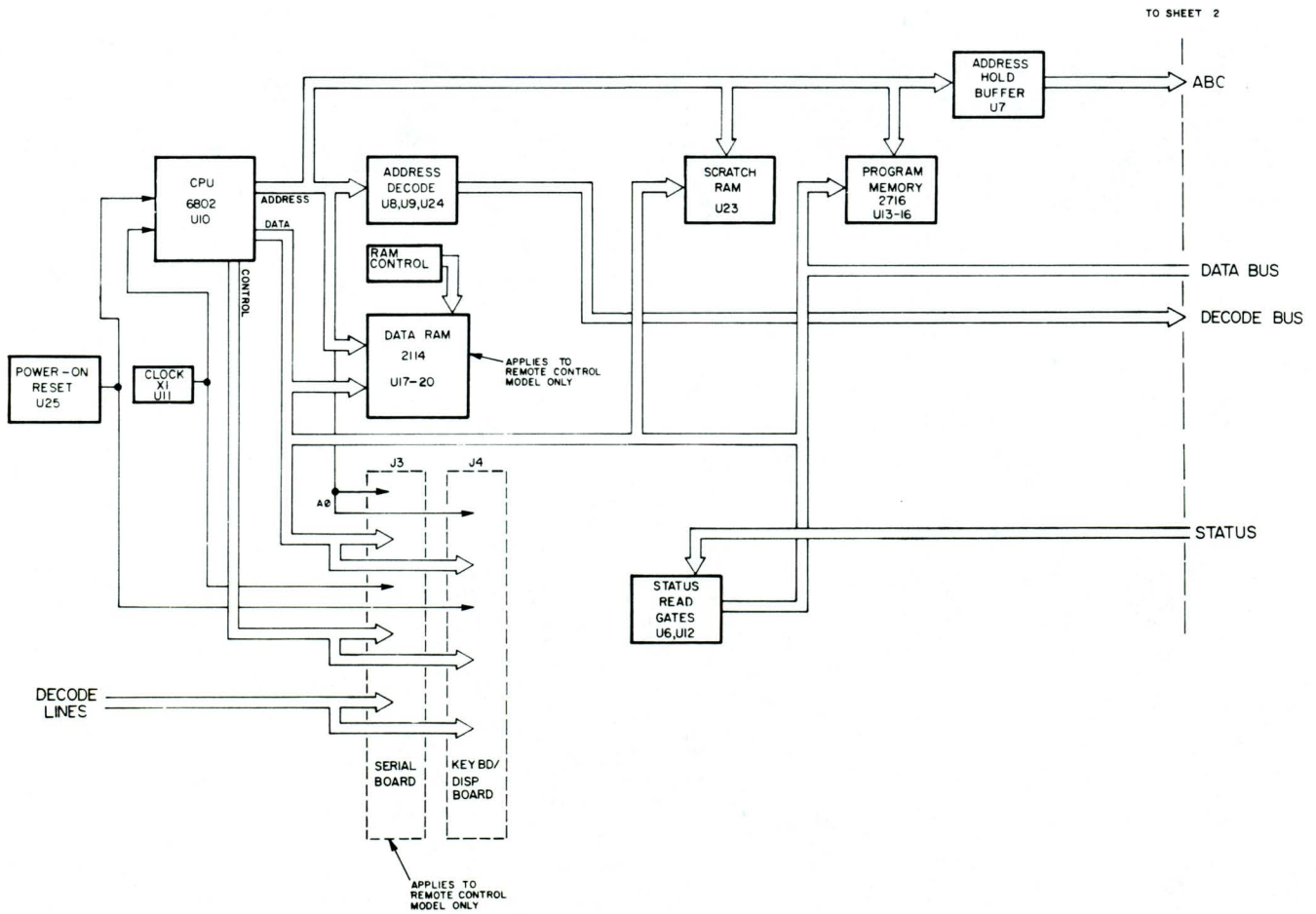


Figure 7-4. Block Diagram, Program Control Board (Sheet 1 of 2)

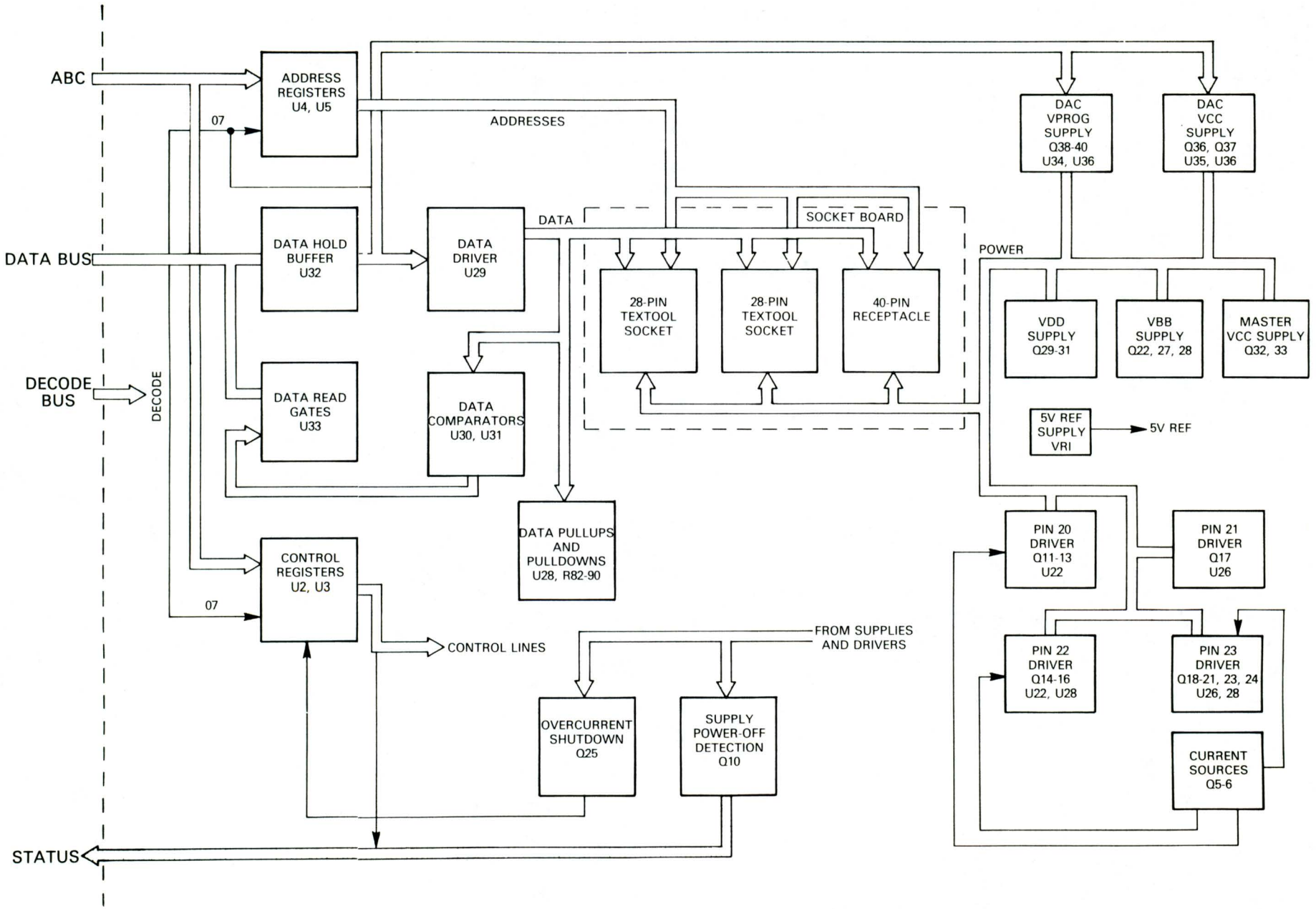


Figure 7-4. Block Diagram, Program Control Board (Sheet 2 of 2)

7.5.3 KEYBOARD/DISPLAY BOARD

Refer to Figure 7-5.

The Keyboard/Display Board (702-0071-001) uses an 8279 keyboard/display interface (U3). The processor writes display information to the 8279 and reads key-switch data directly from it. One set of signals out of the 8279 drives the segments of a 4-digit, 7-segment display (DS2-DS5) through segment drivers U1 and U2. Another set of signals, scan lines SLØ-SL3, are routed through the scan drivers (U4) and applied to the key switches (S1-S3) and the digit drivers (Q1-Q4). The key-switch output is returned to and sensed by the 8279. The scan lines are also applied through the digit drivers to the 7-segment display and are synchronized with the segment lines to scan each digit on a 25% duty cycle.

7.5.4 SOCKET BOARD

Refer to the schematic in Section 9.

The Socket Board (702-0093) houses 2 zero-insertion-force sockets and a receptacle for a 40-pin socket adapter and routes signals from the Program Control Board to the proper socket pins. The board also contains noise-supression circuitry to eliminate spurious programming.

7.5.5 SERIAL I/O BOARD

Refer to Figure 7-6.

The Serial I/O Board (702-0066-001) uses a 6850 serial interface adapter, U9, to produce RS232-compatible signals at serial port J1. Baud rate timing for the 6850 is generated by dividing a clock signal. A 10-segment DIP switch, U4, is used to select the desired baud rate, parity and stop bits. The parity and stop bit segments of the switch are accessed by the processor through the read gates.

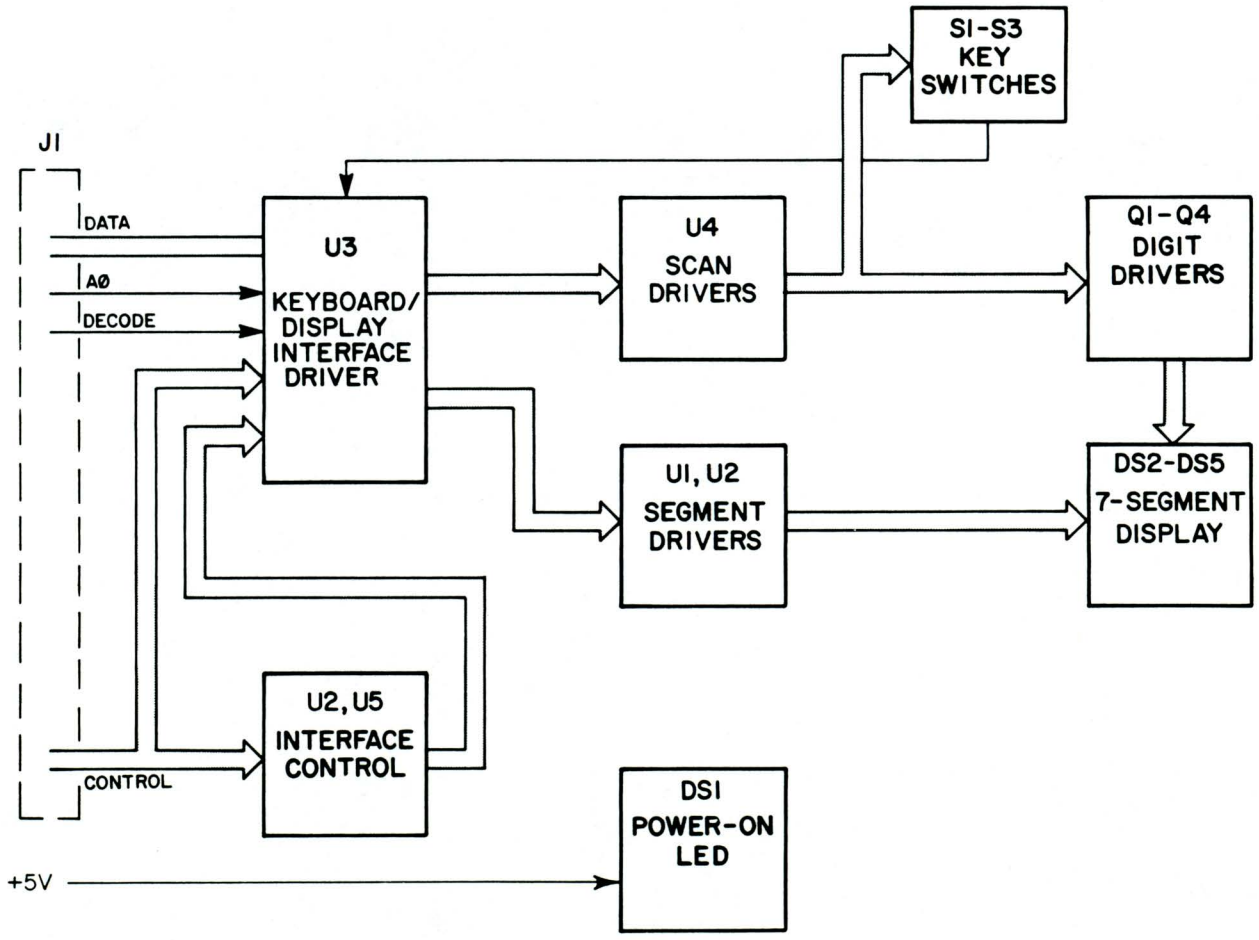


Figure 7-5. Block Diagram, Keyboard/Display Board

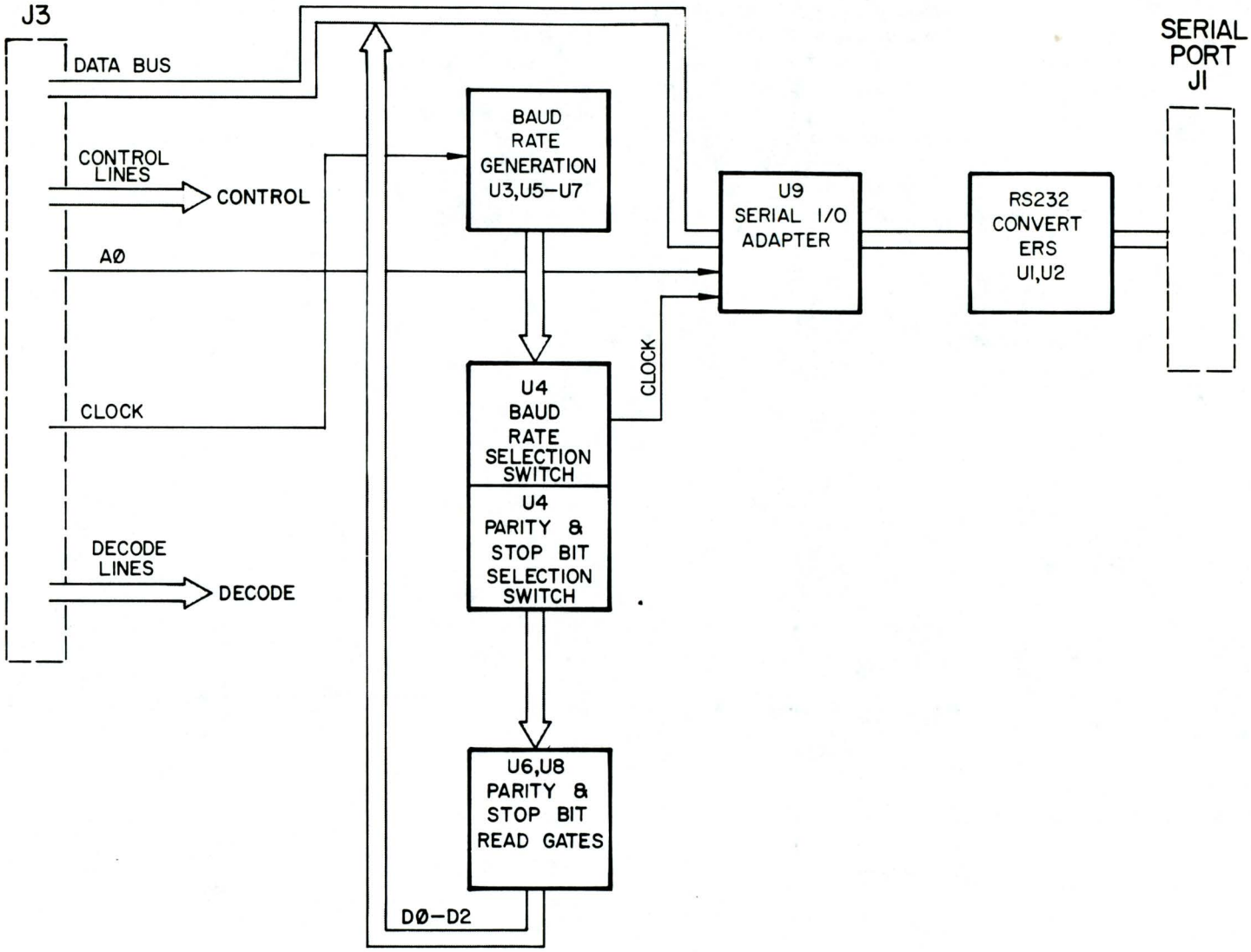


Figure 7-6. Block Diagram, Serial I/O Board

SECTION 8
GLOSSARY

The following terms describe operations which are common in PROM programming.

Blank Check. A routine performed by a programmer to verify that a PROM has no programmed bits, or is "blank." A blank VOL device has ones at every address location; a blank VOH device has zeros.

Programmed Bit. Any "1" found in a VOH device or any "0" found in a VOL device.

Illegal-Bit Check. A routine performed by a programmer to verify that a PROM or other programmable device has no programmed bit that is different from the corresponding bit in RAM. A PROM that fails a blank check may pass an illegal-bit check and still be usable. For example, a VOL PROM you wish to program failed the blank check because of a programmed bit at location 2 of address 13B (see Figure 8-1). If the RAM data contains a "0" at location 2 of address 13B, you can still program the PROM. If location 2 in RAM contains a "1", the PROM bit is illegal and the PROM is not usable.

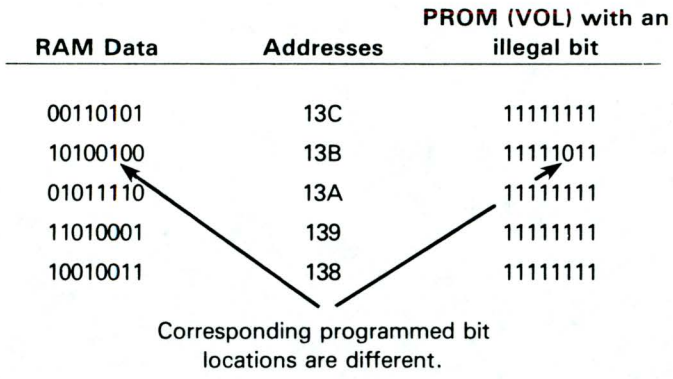


Figure 8-1. Illegal PROM Bit

Sum-check. A binary summation of bits, usually expressed as a 4-digit hex number (16 bits); any carry from the most significant bit is discarded. See Figure 8-2.

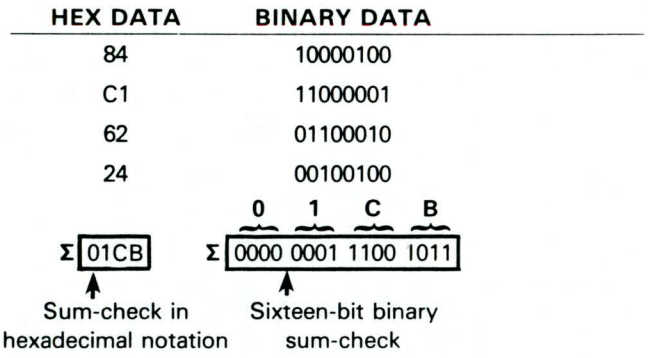
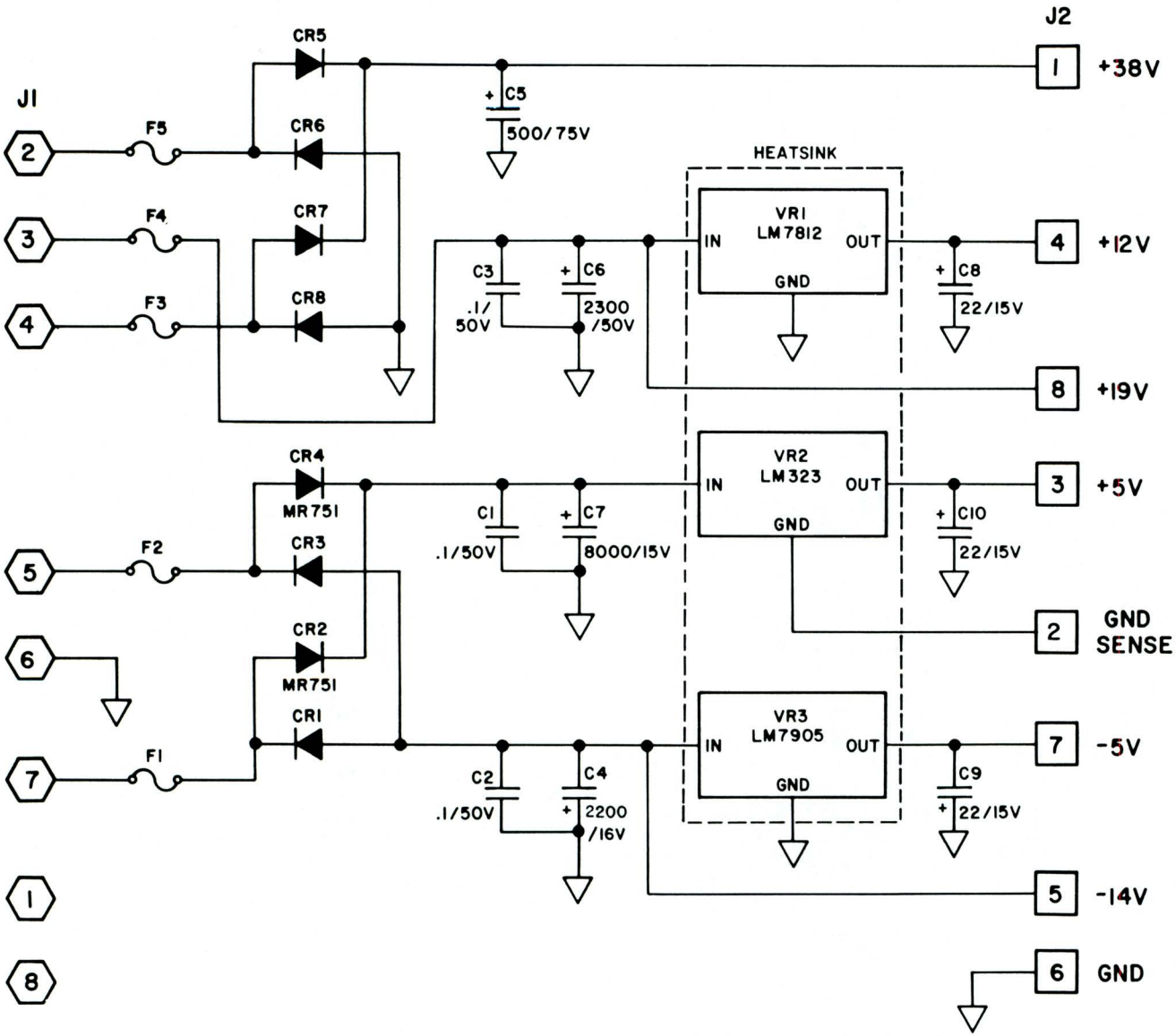


Figure 8-2. Calculation of the Sum-Check of two Eight-Bit Bytes (four hex digits).

SECTION 9
SCHEMATICS

30-702-0072-001	Power Supply Board
30-702-0065-003 (3 pages)	Program Control Board
30-702-0071-001	Keyboard/Display Board
30-702-0093-001	Socket Board
30-702-0066-001	Serial I/O Board (Sheet 1 of 3)

REVISIONS				
ZONE	LTR	DESCRIPTION	PE.	DATE
	A	RELEASE		7-17-80
	B	ECN #3896		1-7-81



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS ARE IN MICROFARADS
2. ALL DIODES ARE IN5392
3. ALL FUSES ARE 2A FAST BLOW
4. SCHEMATIC FOR -001 SHOWN

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O ISSAQUAH, WASH.
PROJ. ENGR. 9/15	TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM POWER SUPPLY
ENG. MGR. 9-15-80		
Q.C. 9/15/80	DRAWN BY: Kathye Hanz	SIZE C · CODE IDENT. NO. 54193 · DRAWING NO. 008-0072
DATE 7-17-80	CHECKED BY: Kathye Hanz	SCALE NONE · SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	CM.	PE	DATE
	A	RELEASE			9/16/80
	B	ECN 3879			12-3-80
	C	ECN 3965			2-3-81
	D	ECN 4099			7-81
	E	ECN 4204			8-81

DATA BUS SHT. 3-1A

BEN SHT. 3-1C

U32 74LS373 — DATA HOLD BUFFER

U33 74LS244 9800 — DATA READ GATES

U29 74LS374 8038 — DATA DRIVER

U6 74LS04

DATA PULLUP/ PULLDOWN

R82 R83 R84 R85 R86 R87 R88 R89 33K (8 PLACES)

CR39 CR38 CR37 CR36 CR35 CR34 CR33 CR32 IN4148 (8 PLACES)

DIODE PROTECTION NETWORK

RP1 RP2 RP3 RP4 RP5 RP6 RP7 RP8 3.3K (8 PLACES)

DATA COMPARATORS

LM339 (8 PLACES)

R91 15K

R94 100K

7407 RS2 2.2K

R93 6.2K

U1 7406

DIODE PROTECTION NETWORK

CR1 CR2 CR3 CR4

CR7 CR8 CR9 CR10 CR11 CR12 CR13 CR14

TP1

CONTROL BUS A SHT. 2-8B

U4 74LS259 8008 — HO ADDRESS REG.

U5 74LS259 8000 — LO ADDRESS REG.

ABC SHT. 2-8C SHT. 3-1B

D7 SHT. 2-8C

OVC RD SHT. 3-3A

CODE J8 SHT. 3-1C

CONTROL BUS B SHT. 2-8A

R90 220 MVcc

U34 AD7524 8020 — VPROG SUPPLY

U35 AD7524 9000 — VCC SUPPLY

LM148

R102 4.99K 1%

R105 4.99K 1%

R107 14.3K 1%

C38 100pf

C39 100pf

C41 .01

R101 28.0K 1%

R103 10K 10T

R108 2.2K

R104 100

R112 100

R110 1.5

R111 1K

R109 10K

R113 3.3

R114 1K

R115 1K

R116 2.2

R117 20K

C37 .1/50V

Q38 MJE240 HEATSINK

Q39 2N2484

Q40 2N2907A

Q36 2N2907A

Q37 MJE 240 HEATSINK

+38 +30 +19 +5 -5 -9

Vref SHT. 2-4D

VProg SHT. 1-5B SHT. 2-6C SHT. 2-6D

VBBCL SHT. 2-2B

CURRENT SENSE SHT. 2-B2

CR42 IN4148 — POWER OFF DETECT SHT. 2-1A

R121 2.2K

Vcc SHT. 2-4B

POWER DISTRIBUTION

R119 1K R120 1K

CR51 CR50 CR49 CR48 CR47 CR46 IN751 (6 PLACES)

C43 1/50V

C1,2,5,8-12,17,20,22,30,31,34-36,40,41,18 .01/100V

C4 C19 47/6V

CR43 IN4734A 5.6V

CR45 IN4734A 5.6V

CR41 IN4739A

R118 120 1/2W

C44 1/35V

TP3

J5: 1 +38; 2 +19; 3 +5V; 4 +12; 5 -14; 6 GND; 7 -5V

CR44 IN4745A 16V

SENSE SHT. 3-4C — R35 5.1 — GND SENSE

J1: D0 D1 D2 D3 D4 D5 D6 D7 VPP

J2: A8 A9 P27DRVR P2DRVR A7 A6 A5 A4 A3 A2 A1 A0 M20 DRVR M22 DRVR

CR19 IN4003 — A1 VProg SHT. 1-3C SHT. 2-6C SHT. 2-6D

CR6 CR5 +5V

NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITOR VALUES ARE MICROFARADS/VOLTS.
3. ALL DIODES ARE IN4148.
4. LAST REFERENCE DESIGNATOR USED:

C44	RP1	CR51
DS3	TP4	
Q40	U36	
R121	VR1	

5. SERIES ZENER DIODES, CR46-51 ARE REQUIRED FOR TEMP. STABILITY.
6. SCHEMATIC FOR -001 SHOWN.
7. FOR -002, DELETE U17-20 AND DS1-DS3.
8. FOR -003, DELETE DS1-DS3 ONLY.

APPROVALS: MFG ENG 9/15; PROJ. ENG. 9/15; ENG. MGR. 9/15/80; Q.C. 9/15/80; DATE 7-28-80

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: DECIMALS .X ±, .XX ±, .XXX ±; ANGULAR ±. DO NOT SCALE DRAWING.

DRAWN BY: J OBIE

CHECKED BY:

DATA I/O ISSAQUAH WASH

TITLE: SCHEMATIC DIAGRAM PROGRAM CONTROL BD

SIZE	CODE IDENT NO	DRAWING NO
D	54193	008-0065

SCALE — SHEET 1 OF 3

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE	DATE
		SEE SHEET 1			

CONTROL REGISTERS

CODE BUS SHT.3-1C

D7 SHT.1-8B

ABC SHT. 3-1B SHT.1-8B

U2 74LS 259 8018

U3 74LS 259 8010

PIN 20 DRIVER

PIN 22 DRIVER

PIN 23 DRIVER

PIN 21 DRIVER

J1 PIN 20 DRVR

J1 PIN22 DRVR

J1 PIN23 DRVR

J2 PIN 21 DRVR

J2 M 23 DRVR

CATHODES

J2 MVcc

CONTROL BUS A SHT.1-6B

CONTROL BUS B SHT.1-8A

OVC RD SHT.3-3A

SOCKET POWER IND

PROG/ERROR IND

MASTER 23 DRIVER

AC POWER IND

CURRENT SOURCES

VDD SUPPLY

VBB SUPPLY

OVERCURRENT SHUTDOWN

5 VOLT REFERENCE SUPPLY

MASTER Vcc SUPPLY

SUPPLY POWER OFF DETECT

SUP RD SHT.3-2A

CURRENT SENSE SHT. 2-2C

VBBCL SHT.1-3C

POWER OFF DETECT SHT.1-3C

Vref SHT. 1-4C

Vcc SHT.1-4B

VProg SHT.1-3C

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O ISSAQUAH WASH.	
PROJ. ENG.	TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM PROGRAM CONTROL BD	
ENG. MGR.			
Q.C.	DRAWN BY G. Ryder	SIZE D	CODE IDENT NO 54193
DATE 7-28-80	CHECKED BY:	SCALE NONE	SHEET 2 OF 3

REVISIONS				
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		SEE SHEET 1			

PROCESSOR

ADDRESS DECODE

SCRATCH RAM

PROGRAM MEMORY

POWER ON RESET

DECODE BUS SHT. 2-8D SHT. 1-8A

BEN SHT. 1-8C

ABC SHT. 1-8B SHT. 2-8C

ADDRESS HOLD BUFFER

DATA RAM

DATA BUS SHT. 1-8D

SUP RD SHT 2-4A

OVC RD SHT. 2-8B

CLOCK

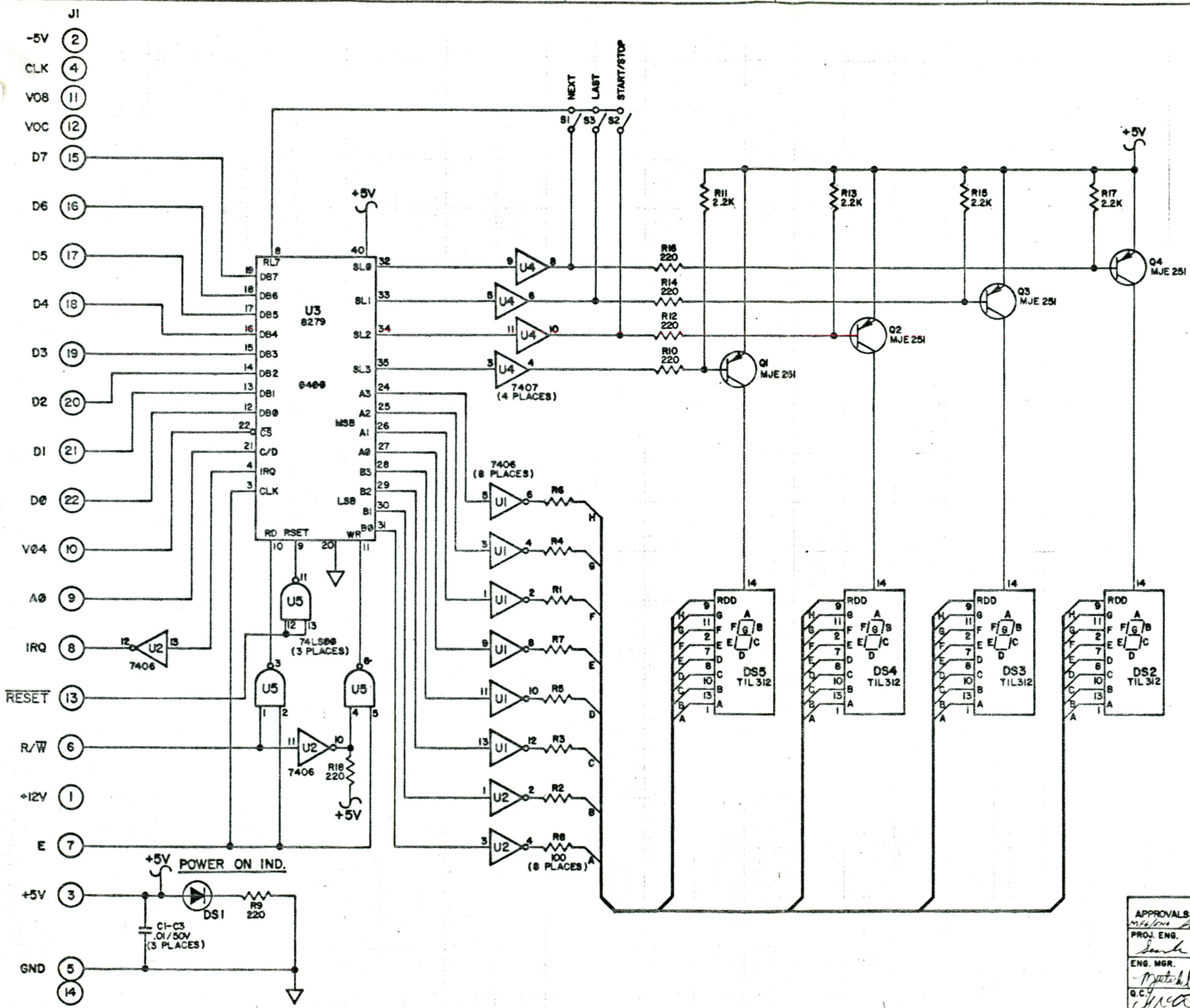
STATUS READ GATES

J3 SERIAL BD

J4 KB/DISP BD

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O ISSAQUAH, WASH
PROJ. ENG.	TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM PROGRAM CONTROL BD.
ENG. MGR.		
Q.C.	DRAWN BY: T.CONNERTON	SIZE D · CODE IDENT NO 54193 · DRAWING NO 008-0065
DATE 7/24/80	CHECKED BY:	SCALE · SHEET 3 OF 3

REVISIONS					
ZONE	LTR	DESCRIPTION	CM	PE	DATE
	A	RELEASE			10-1-80



NOTES- UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED:
   - R18 DS5
   - U5 J1
   - C3 Q4
4. SCHEMATIC -001 SHOWN.

NOT SHOWN		
DEVICE	+5V	GND
U1	14	7
U2	14	7
U4	14	7
U5	14	7

APPROVALS: M.F. 10-1-80	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O BRAQUIAN, WASH.	
PROJ. ENG. Scott 10-1-80	TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM KEYBOARD/DISPLAY	
ENG. MGR. 10-3-80			
Q.C. 10-3	DRAWN BY 7/23/80 G. Ryder	SIZE D	CODE IDENT NO. 54193
DATE 10-1-80	CHECKED BY:	SCALE NONE	DRAWING NO. 008-0071 SHEET 1 OF 1

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	S.N.	KM	[illegible]	7-29-81

P102: A0 A1 A2 A3 A4 A5 A6 A7 P2 P27 A8 A9 GND M20 M22 VCC GND P21 MVCC M23 — pins 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

U1 MASTER SOCKET

U2 COPY SOCKET

C2 .1/50V

C1 .1 50V

C3 .1/50V

CR4

CR3

CR2

CR1

J104

A3	1
A2	2
A1	3
A0	4
P2	5
P27	6
M23	7
D1	8
D2	9
D3	10
D4	11
D5	12
D6	13
D7	14
D8	15
GND	16

J103

1	A4
2	A5
3	A6
4	A7
5	A8
6	A9
7	GND
8	VCC
9	MVCC
10	M20
11	M22
12	P20
13	P22
14	P23
15	P21
16	VPP

P101: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 — D1 D2 D3 D4 D5 D6 D7 D8 GND GND GND VPP GND P23 GND P22 GND P20 GND CATHODES

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS ARE IN MICROFARADS.
2. LAST REFERENCE DESIGNATOR USED: CR4, C3, U2
3. ALL DIODES ARE IN4148
4. 702-0093-001 SHOWN

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.		DATA I/O ISSAQUAH, WASH
DSN. ENGR.	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR		TITLE: SCHEMATIC DIAGRAM 20B SOCKET BOARD
MFG. ENGR.	DATE			
QUAL. ASSUR.	DATE	DRAWN BY: SUENEE H.	DATE: 6-81	SIZE: D; CODE INDENT. NO.: 54193; DRAWING NO.: 30-702-0093
ENGR. MGR.	DATE	CHECKED BY:	DATE	SCALE: NONE; SHEET: 1 OF 1

DRWING #9270

REVISIONS				
ZONE	LTR	DESCRIPTION	CM.	PE	DATE
	A	RELEASE			7-17-80

J3

D7 15 7
D6 16 6
D5 17 5
D4 18 4
D3 19 3
D2 20 2
D1 21 1
D0 22 0
A0 9
R/W 6
IRQ 8
E 7
CLK 4
V04 10
V08 11
88 13
+12V 1 +12V
-5V 2 -5V
+5V 3 +5V
GND 5
14

C1-6 .01/50V

BAUD RATE GENERATION

+5V
U5 74LS161 CLR 1, B 4, C 6, D 7, PEN 10, TEN; CLK 2; QC 12, LD 9, CY 15, A 3
U6 74LS04
R3 10K
R2 10K
U4
U3 4040 Q1 9, Q2 7, Q3 6, Q4 5, Q5 3, R 11
10 POS. DIP SW
ISB 13, ON 12, PARITY, EVEN 11
R6 R5 R7 10K(3PLCS)
U6 74LS04
U8 74LS126(3PLCS)
U7 74LS161 QD 11, CLK 2, LD 9, CLR 1, PEN 7, TEN 10, CY 15, A 4, B, C 5, D 6
U6 74LS04

U9 6850
CS2 9, CS1 8, CS0 10, VCC 12 +5V
CTS 24, RX 2, TX 6, RTS 5
D7 15, D6 16, D5 17, D4 18, D3 19, D2 20, D1 21, D0 22
RS 11, R/W 13, IRQ 7
ETX CLK 4, RX CLK 3

SERIAL PORT

U2 1489 3 → 1 → R4 10K +5V → J1 5 CTS
U2 1489 11 → 13 → J1 3 RX
U1 1488 12, 13 → 11 → J1 2 TX
U1 1488 2 → 3 → J1 4 RTS
J1 1 GND
J1 7

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED: RT, C6, U10
4. SCHEMATIC FOR -001 SHOWN

NOT SHOWN

GND		+5V	
U2	PIN 7	U2	PIN 14
U3	8	U3	16
U5	8	U5	16
U6	7	U6	14
U7	8	U7	16
U8	7	U8	14

UNUSED GATES:

+5V
U6 1, 2; U6 5, 6; U6 11, 10

74LS04

-001 SHOWN

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O ISSAQUAH WASH
PROJ. ENG. 9/15	TOLERANCES: DECIMALS X ±, XX ±, XXX ±; ANGULAR ±; DO NOT SCALE DRAWING	TITLE: SCHEMATIC DIAGRAM — SERIAL I/O BOARD
ENG. MGR. 9-15-80	DRAWN BY: Jaehee Kim	SIZE D; CODE IDENT NO 54193; DRAWING NO 008-0066
Q.C. 9/15/80	CHECKED BY:	SCALE NONE; SHEET 1 OF 3
DATE 7-17-80		

APPENDIX A
DATA TRANSLATION FORMAT SPECIFICATIONS

A.1 INTRODUCTION

This section gives the specifications of the translation formats available for input and output by the Model 20B. The Select Codes for each of the formats are listed in Table A-1.

Table A-1. Select Codes for Translation Formats

FORMAT	SELECT CODE
Binary	10
ASCII-Hex Space	50
MOS Technology	81
Motorola Exorciser	82
Intel Intellec 8/MDS	83
Tektronix Hexadecimal	86

A.2 BINARY TRANSFER, Select Code 10

Data transfer in the Binary format consists of a stream of 8-bit data words preceded by a byte count and followed by a sum-check. The Binary format does not have addresses.

A tape generated by the programmer will contain a 5-byte, arrow-shaped header followed by a null and a 4-nibble byte count. The start code, a nonprintable rubout in even parity, follows the byte count. The end of data is signalled by two nulls and a 2-byte sum-check of the data field.

A.3 INPUT REQUIREMENTS

The programmer stores incoming binary data upon receipt of the start character. Data is stored in RAM sequentially starting at the Begin RAM Address and ending at the last incoming data byte. Transmission may be aborted by pressing START/STOP.

For binary tapes with no byte count or sum-check, the number of bytes to be transmitted must be set, in order to indicate the end of transmission. (This must be done by setting the Set Block Size command in remote control.) These tapes use a rubout code (FF) to signal start and do not use the arrow-shaped header.

A.4 OUTPUT CHARACTERISTICS

Hard copy from binary files is not useful because the terminal interprets output from the programmer as ASCII characters. Output can be used to produce binary tapes.

Programmer output in binary consists of a sequential data stream preceded by the arrow-shaped header, one null, byte count and start code and followed by 2 nulls and a sum-check. As with Input, transmission may be aborted by pressing START/STOP.

A.5 ASCII-HEX SPACE FORMAT Select Code 50

This format has a start and end code. The ASCII-Hex Space start code is an STX.

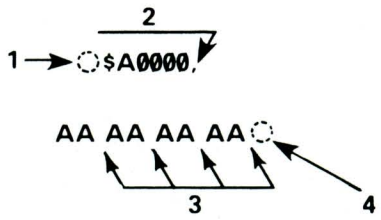
A.5.1 INPUT REQUIREMENTS

Figure A.1 illustrates four data bytes coded in ASCII-Hex Space. Data in this format is organized in sequential bytes separated by the space character. Characters immediately preceding the space character are interpreted as data. Data bytes are expressed by 2 hex characters. Line feeds, carriage returns and other characters may be included in the data stream as long as a data byte directly precedes each space character.

Although each data byte has an address, most addresses are unexpressed. Data bytes are addressed sequentially unless an explicit address is included in the data stream. This address is preceded by a "$" and an "A", must contain 2 to 4 hex characters, and must be followed by a comma. The programmer skips to the new address to store the next data byte; succeeding bytes are again stored sequentially. See Figure A.2.

This format has an end code, ETX, which terminates input operations. However, if a new start code follows within 16 characters of an end code, input will continue uninterrupted.

ASCII-Hex Space, Select Code 50



NOTES

1. **Start code is nonprintable STX -CTRL B HEX 02.**
2. **Optional address code may precede any data byte. Up to four address digits in hex digits.**
3. **Execute code (space).**
4. **End code is a nonprintable ETX -CTRL C or HEX 03.**

Figure A.1. ASCII-Hex Space Format

After receiving the final end code following an input operation, the programmer calculates a sum-check of all incoming data. Optionally, a sum-check can also be entered in the input data stream. The programmer compares this sum-check field with its own calculated sum-check. If they match, the programmer will simply display the sum-check; if they do not match, the programmer will display a sum-check error. Specifications for the optional sum-check field are given in Figure A.3.

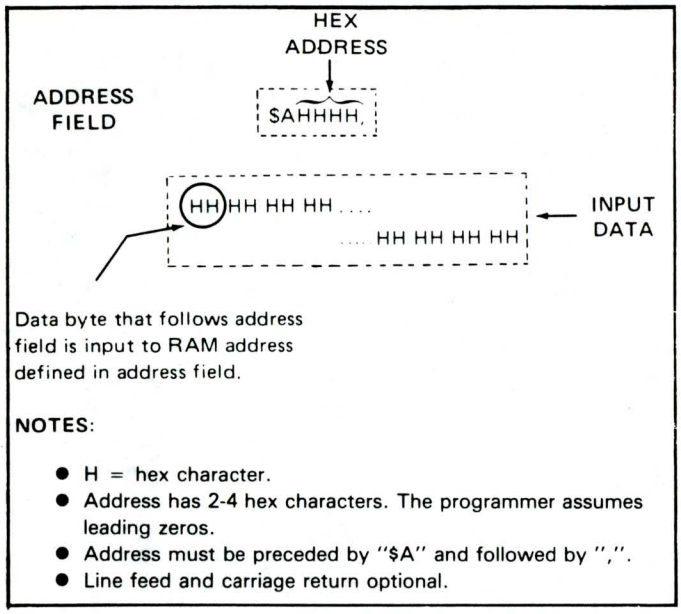


Figure A.2. Optional Address Field in ASCII-Hex Space Format.

A.5.2 OUTPUT CHARACTERISTICS

Data is output from the programmer between the address limits set by the Begin RAM Address and the number of bytes to be transferred. After these parameters have been set, output is begun by invoking the Output command. The programmer divides output data into eight-line blocks.

Data transmission is begun with the start code, a nonprintable STX. Data blocks follow, each one prefaced by an address for the first data byte in the block. The end of transmission is signaled by the end code, a nonprintable ETX. Directly following the end code is a sum-check of the transferred data. The transmission is preceded and followed by fifty null characters.

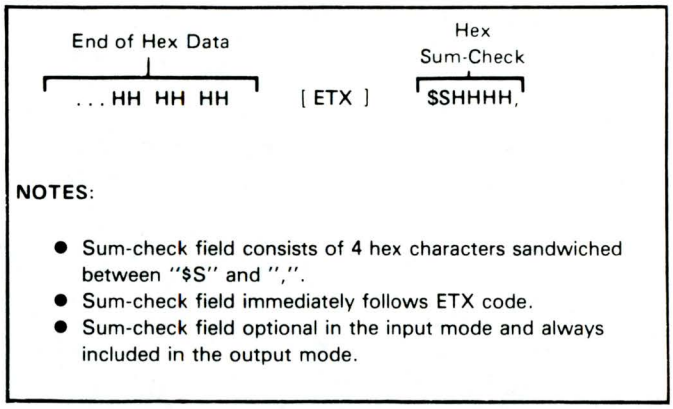


Figure A.3. Syntax of the Sum-Check Field in I/O Operations

A.6 MOS TECHNOLOGY FORMAT
Select Code 81

The data in each record is sandwiched between a seven-character prefix and a four-character suffix. The number of data bytes in each record must be indicated by the byte count in the prefix. The input file can be divided into records of various lengths.

Figure A.4 simulates a series of valid data records. Each data record begins with a semicolon (;). The programmer will ignore all characters received prior to the first semicolon. All other characters in a valid record must be valid hex digits (0-9, A-F). A two-digit byte count follows the start character; the byte count, expressed in hexadecimal digits, must equal the number of data bytes in the record. The next four digits make up the address of the first data byte in the record. Data bytes follow, each represented by two hexadecimal digits.

The suffix is a four-character checksum, which represents the sixteen-bit binary sum of all hexadecimal bytes in the record, including the address and byte count. Carry from the most significant bit is dropped.

A.6.1 OUTPUT CHARACTERISTICS

Data is output from the programmer, starting at the Begin RAM Address and continuing until the number of bytes in the specified block has been transmitted.

Output is begun by invoking the Output command.

The programmer divides output data into records prefaced by a start character and by an address field for the first data byte in the record. The transmission is preceded and followed by fifty null characters.

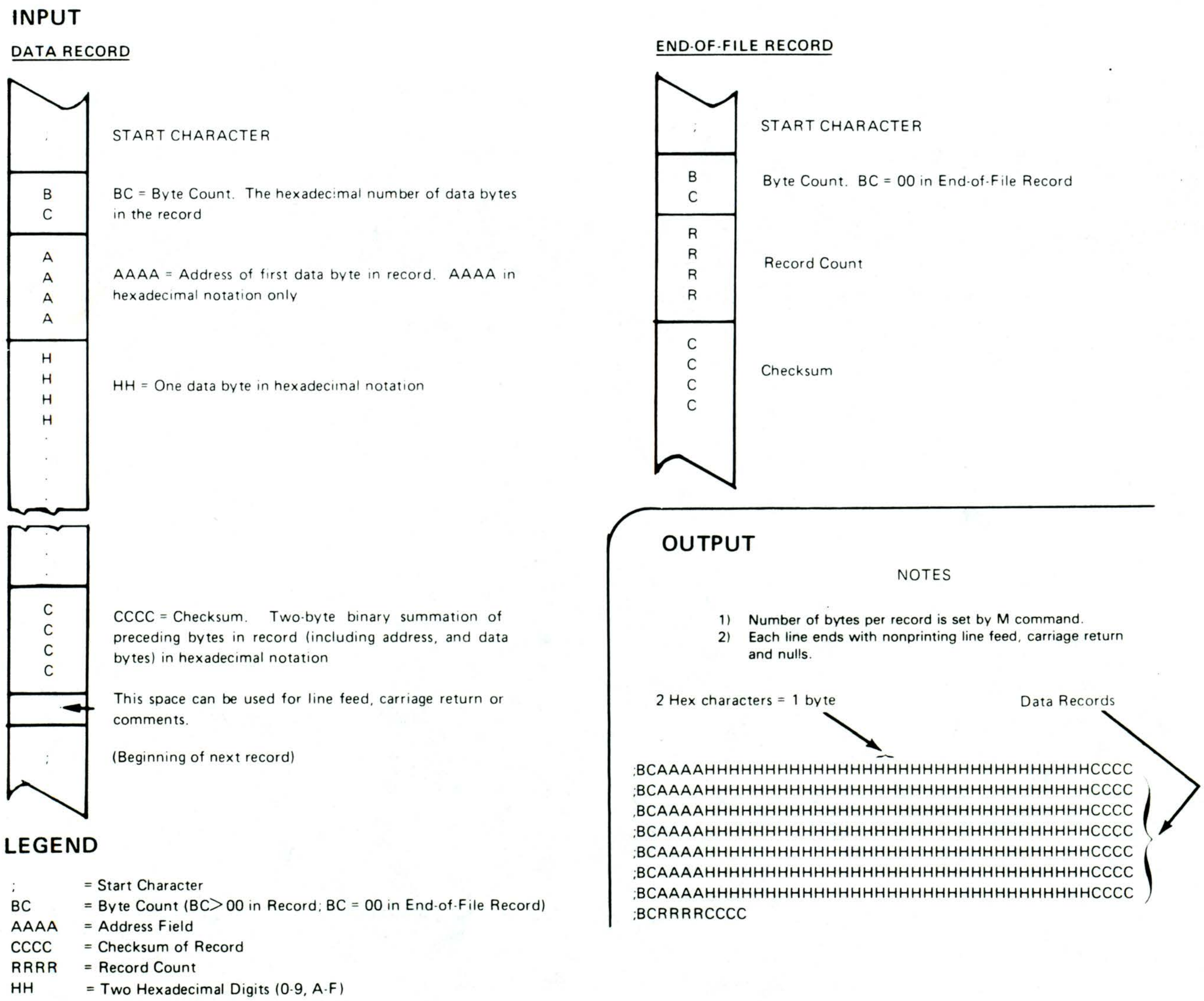


Figure A.4. Specifications for Valid MOS Technology Data Files

A.7 MOTOROLA EXORCISER FORMAT
Select Code 82

Motorola data files may begin with an optional sign-on record, which is initiated by the code SØ. Valid data records start with an eight-character prefix and end with a two-character suffix. Figure A.5 demonstrates a series of valid Motorola data records.

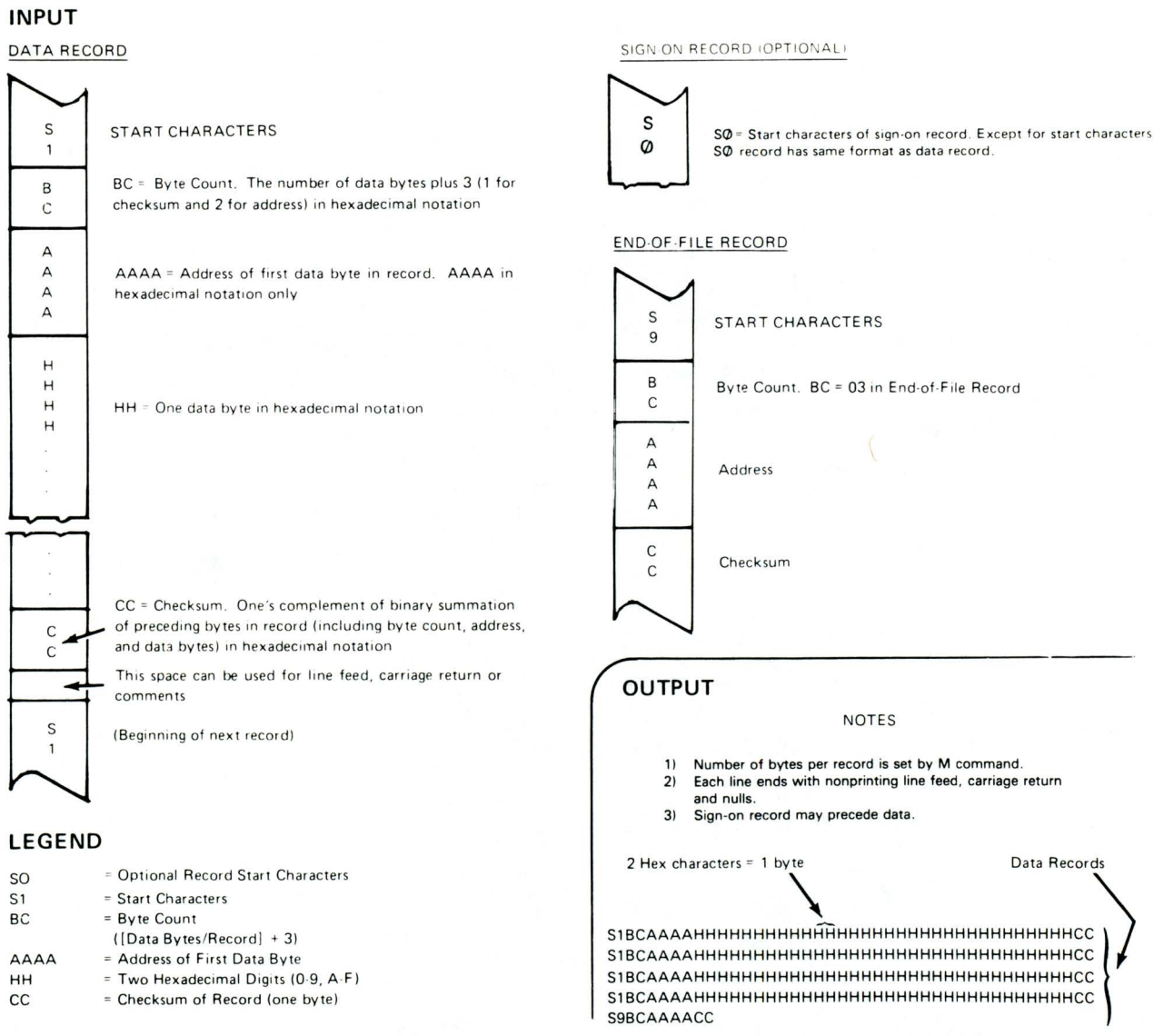
Each data record begins with the start characters, "S1"; the programmer will ignore all earlier characters. The third and fourth characters represent the byte count, which expresses the number of data, address and checksum bytes in the record. The address of the first data byte in the record is expressed by the last four characters of the prefix. Data bytes follow, each represented by two hexadecimal characters. The number of data bytes occurring must be three less than the byte count. The suffix is a two-character checksum.

A.7.1 OUTPUT CHARACTERISTICS

Data is output from the programmer, starting at the Begin RAM Address and continuing until the number of bytes in the specified block has been transmitted.

Output is begun by invoking the Output command.

The programmer divides output data into records prefaced by a start character and by an address field for the first data byte in the record. The transmission is preceded and followed by fifty null characters.



LEGEND

SO	= Optional Record Start Characters
S1	= Start Characters
BC	= Byte Count ([Data Bytes/Record] + 3)
AAAA	= Address of First Data Byte
HH	= Two Hexadecimal Digits (0-9, A-F)
CC	= Checksum of Record (one byte)

Figure A.5. Specifications for Valid Motorola Data Files

A.8 INTEL INTELLEC 8/MDS FORMAT
Select Code 83

Intel data records begin with a nine-character prefix and end with a two-character suffix. The byte count must equal the number of data bytes in the record.

Figure A.7 simulates a series of valid data records. Each record begins with a colon (:), which is followed by a two-character byte count. The four digits following the byte count give the address of the first data byte. The address is followed by a two digit record type.

Each data byte is represented by two hex digits; the number of data bytes in each record must equal the byte count.

The suffix is a two-digit checksum, the two's complement of the binary summation of the previous bytes in the record.

A.8.1 OUTPUT CHARACTERISTICS

Data is output from the programmer, starting at the Begin RAM Address and continuing until the number of bytes in the specified block has been transmitted.

Output is begun by invoking the Output command.

The programmer divides output data into records prefaced by a start character and by an address field for the first data byte in the record. The transmission is preceded and followed by fifty null characters.

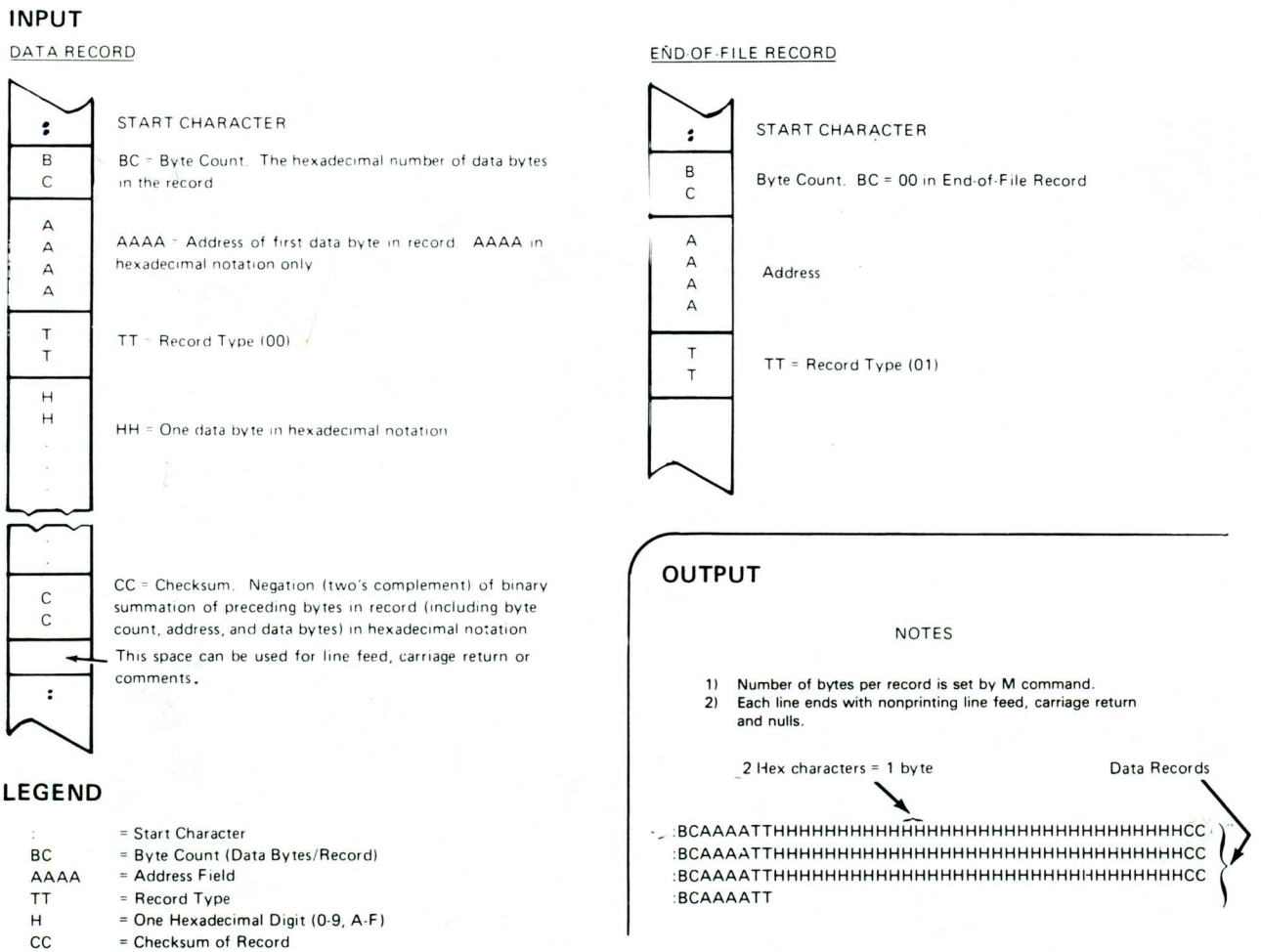


Figure A.6. Specifications for Valid Intel Intellec 8/MDS Data Files

A.9 TEKTRONIX HEXADECIMAL FORMAT Select Code 86

Figure A.7 illustrates a valid Tektronix data file. The data in each record is sandwiched between the start character, a slash (/), and a two-character checksum. Following the start character, the next four characters of the prefix express the address of the first data byte. This address is followed by a byte count, which represents the number of data bytes in the record, and by a checksum of the address and byte count. Data bytes follow, represented by pairs of hexadecimal characters and succeeded by a checksum of the data bytes. The End-of-File record consists only of control characters used to signal the end of transmission, and a byte count and checksum for verification.

If the programmer receives an abort record it will ignore it. An abort contains a start character of two slashes (//), error information and a carriage return.

A.9.1 OUTPUT CHARACTERISTICS

Data is output from the programmer, starting at the Begin RAM Address and continuing until the number of bytes in the specified block has been transmitted.

Output is begun by invoking the Output command.

The programmer divides output data into records prefaced by a start character and by an address field for the first data byte in the record. The transmission is preceded and followed by fifty null characters.

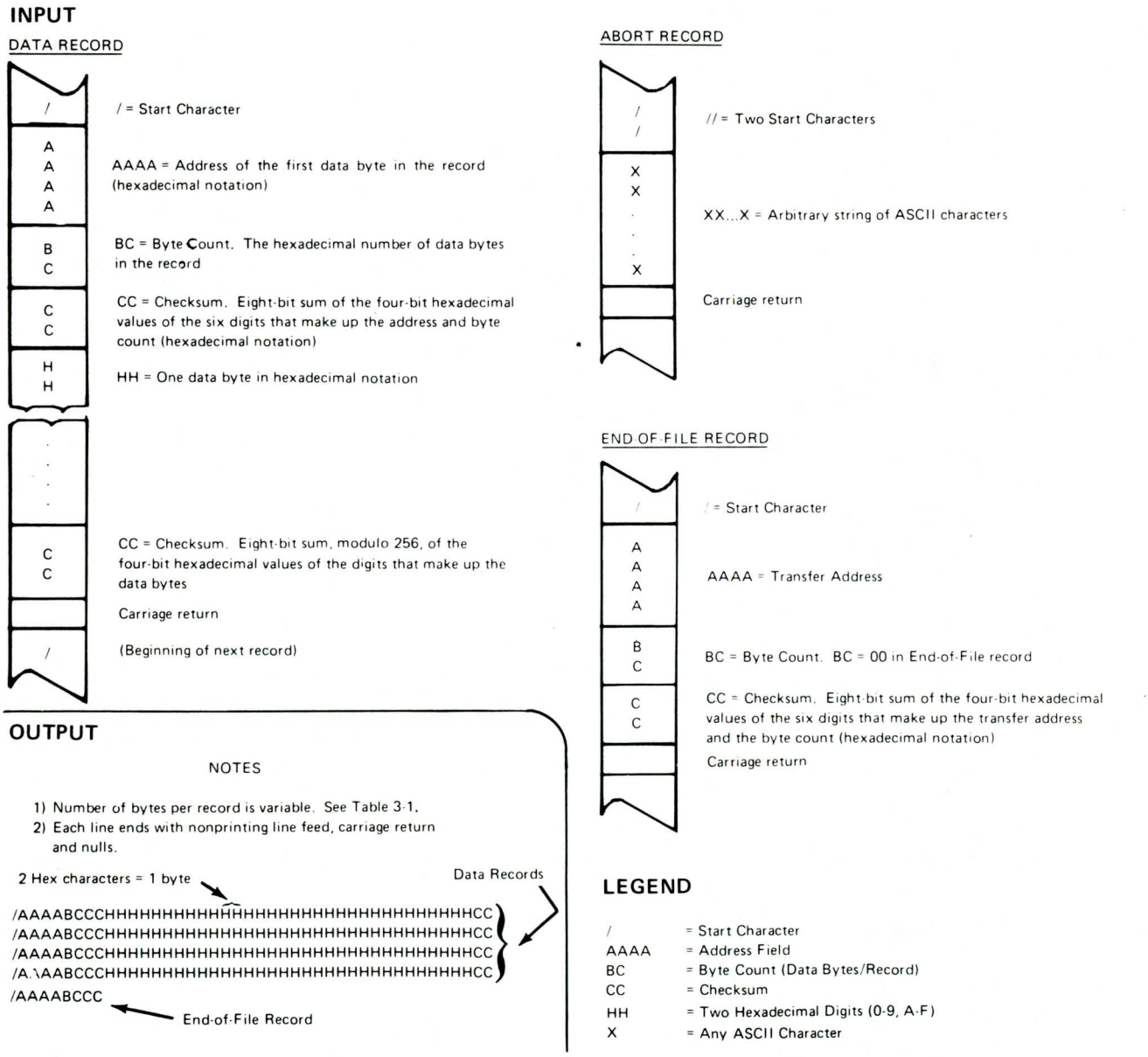


Figure A.7. Specifications for Valid Tektronix Hexadecimal Data Files